VSX104+V2 Manual

PC/104+ x86 CPU module, with IDE, Four Serial ports, Dual Ethernet, USB 2.0, Parallel port and Compact Flash

INTENDED FOR VERSION 2 OF THE PCB ONLY

Manufactured by:
TRI-M ENGINEERING
Engineered Solutions for Embedded Applications

Technical Manual

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PREFACE

This manual is for integrators of applications of embedded systems. It contains information on hardware requirements and interconnection to other embedded electronics.

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CHAPTER 1: GENERAL DESCRIPTION

The VSX104+ is a PC/104+ compliant system controller measuring just 3.55 inches by 3.775 inches. The VSX104+ offers the quickest route of integrating a full x86 AT-compatible computer into your embedded control application using the PC/104+ form factor. In addition, the built-in peripherals minimize the number of additional modules required. By combining the system hardware, I/O, software (integrated OS image) and solid-state mass storage, the VSX104++ lowers your exposure to possible development risks, costs and significantly reduces your time-to-market.

The VSX104+'s full compatibility with the popular PC/104+ embedded expansion bus allows you to easily integrate the widest selection of low-cost hardware peripherals. The numerous features provide an ideal price/performance solution.

1.1 Specifications/Features

1.1.1 Vortex86SX

- Fully 486 compatible core running at 300MHz.
- Six stage pipe-line.
- Integrated 16KB L1 instruction cache, 16KB L1 data cache.

1.1.2 Memory

- On-board 128MB.
- Dual Data Rate II 533MHz.

1.1.3 RS232 Interface

- Four full signaled external RS232 ports.
- All ports support up to 115200 baud.

1.1.4 Universal Serial Bus Interface

- Two ports USB2.0 high speed.

1.1.5 Ethernet Interface

- One on-chip 10/100 BaseT Fast Ethernet Controller.
- One additional Intel 82551er 10/100 BaseT Fast Ethernet Controller.

1.1.6 Parallel Interface

- One enhanced bi-directional parallel port.
- Supports SPP, ECP and EPP.

1.1.7 Keyboard/Mouse Interface

- Supports AT keyboard and PS/2 mouse.

1.1.8 Enhanced IDE Interface

- One enhanced IDE channel, supports up to two drives (master/slave).
- Ultra DMA and PIO modes (1-4) support.

1.1.9 On board backup battery

- Keeps RTC running and CMOS data when the board is unpowered.

1.1.10 Expansion BUS - PC/104+ signals

- Fully compliant 16-bits PC/104 Expansion BUS.
- Fully compliant 32-bits PCI-104 Expansion BUS.

1.1.11 Flash Storage

- On-board Compact Flash socket.
- On-board Micro-SD socket.
- On-board SPI Flash.

1.1.12 Jumperless configuration

- No hardware jumper required.
- Entirely configurable through the BIOS setting.

1.1.13 Software Compatibility

- Linux.
- Windows CE.
- DOS.

1.1.14 Mechanical/Environmental

- PC/104+ form factor compliant, 3.55" x 3.775" x 0.9" (90mm x 96mm x 23mm).
- Standard with PC/104 16-bit stackthrough connector for PC/104-compliant modules.
- Operating temperature: -40° to 185°F (-40° to 85°C).
- Storage temperature: -58° to 257°F (-50° to 125°C).
- Weight 0.12 lb (53 grams).

CHAPTER 2: INSTALLATION

2.1 Locating the connectors

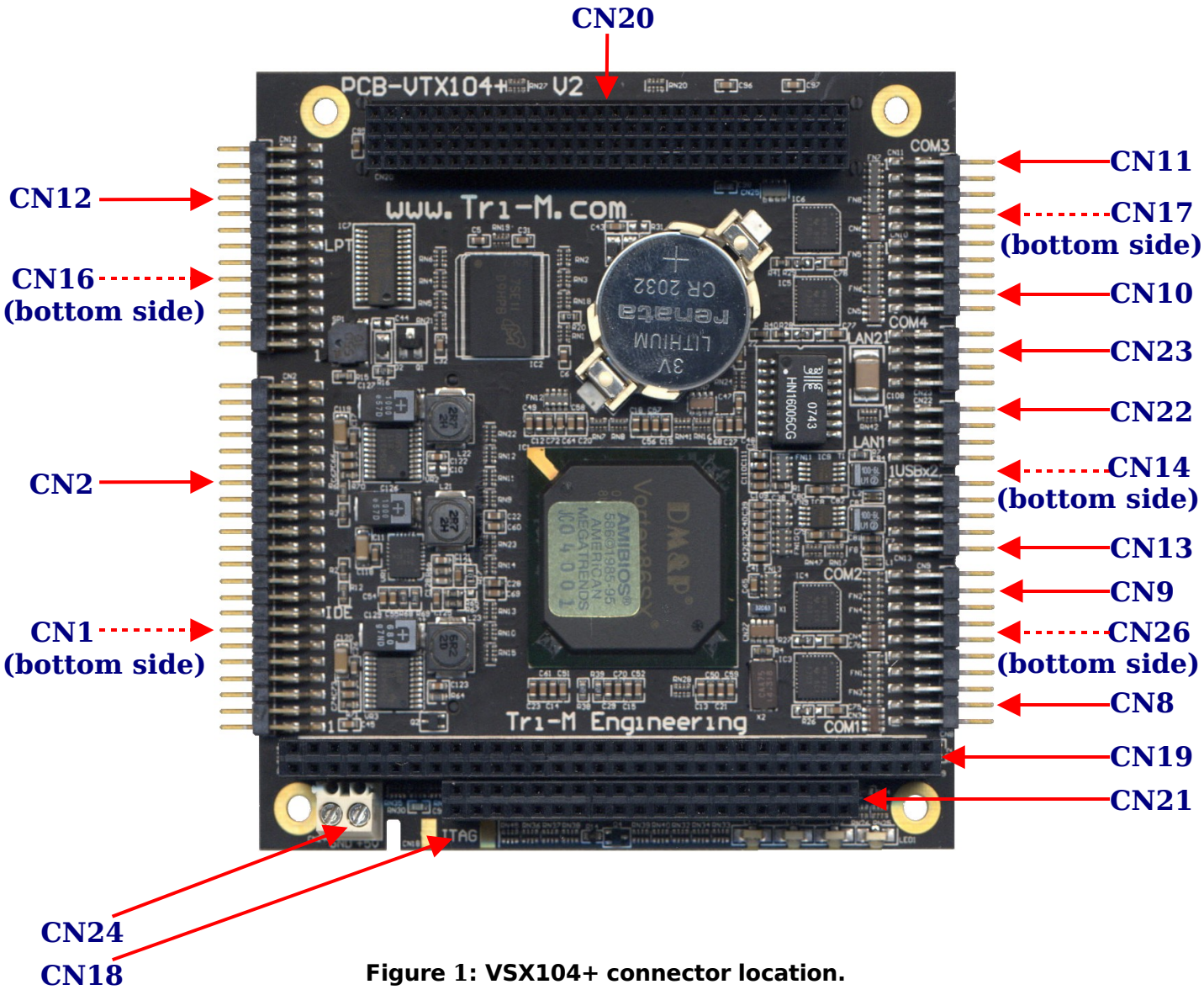


Figure 1: VSX104+ connector location.

CHAPTER 3: JUMPERS

NOT APPLICABLE

The VSX104+ is jumperless, all the configuration is done through software.

CHAPTER 4: CONNECTORS

Connectors on the VSX104+ are provided to interface external devices such as a Compact Flash, hard disk drive, microSD, Serial ports, Parallel port, USB, LAN, SPI, Mouse, keyboard, GPIO...

VSX104+ Connector List	
Connector Label	Function
CN1	Compact Flash socket
CN2	IDE Interface
CN8	Serial port COM1
CN9	Serial port COM2
CN10	Serial port COM4
CN11	Serial port COM3
CN12	Parallel port
CN13	Dual USB 2.0
CN14	MicroSD socket
CN16	Redundancy port
CN17	PS/2 and SPI
CN18	JTAG port
CN19	PC/104 8 bits BUS
CN20	PC/104+ 32 bits BUS
CN21	PC/104 16 bits BUS
CN22	LAN Interface 1
CN23	LAN Interface 2
CN24	Input power +5VDC
CN26	GPIO port 0

Table 1: VSX104+ Connector List

4.1 Compact Flash Socket (CN1)

The VSX104+ embeds a Compact Flash socket directly interfaced to the ATA BUS allowing the Compact Flash to be detected as Hard-drive without additional software driver.
The Compact Flash socket is configured by default as Primary Slave but can be changed to Primary Master through software by reconfiguring the GPIO port 2 bit 2.
The Compact Flash can be used to boot an Operating System or as a storage device.

Compact Flash Socket (CN1)			
Pin #	**Signal**	**Pin #**	**Signal**
1	GND	2	D03
3	D04	4	D05
5	D06	6	D07
7	-CS0	8	NC
9	-ATA SEL	10	NC
11	NC	12	NC
13	Vcc	14	NC
15	NC	16	NC
17	NC	18	A02
19	A01	20	A00
21	D00	22	D01
23	D02	24	NC
25	NC	26	NC
27	D11	28	D12
29	D13	30	D14
31	D15	32	-CS1
33	NC	34	-IORD
35	-IOWR	36	NC
37	INTRQ	38	Vcc
39	-CSEL	40	NC
41	-RESET	42	IORDY
43	-INPACK	44	-REG
45	-DASP	46	-PDIAG
47	D08	48	D09
49	D10	50	GND

Table 2: Compact Flash Interface

4.2 IDE Interface (CN2)

The VSX104+ carries an IDE interface compatible with the ATA/ATAPI-6 specification handling up to two devices, one Master and one Slave (Compact Flash socket included). The interface supports the PIO modes 0 to 4 with flow control, the DMA 0 to 2 and the ultra DMA 0 to 6.

IDE Interface (CN2)			
TOP		**BOTTOM**	
Pin #	**Signal**	**Pin #**	**Signal**
1	HDRESET-	2	GND
3	HDD07	4	HDD08
5	HDD06	6	HDD09
7	HDD05	8	HDD10
9	HDD04	10	HDD11
11	HDD03	12	HDD12
13	HDD02	14	HDD13
15	HDD01	16	HDD14
17	HDD00	18	HDD15
19	GND	20	KEY
21	IDEPDREQ	22	GND
23	HDIOW-	24	GND
25	HDIOR-	26	GND
27	HDRDY	28	GND
29	IDEPDACK	30	GND
31	IRQ14	32	NC
33	HDA1	34	RSVD
35	HDA0	36	HDA2
37	HDCS0-	38	HDCS1-
39	LEDIN-	40	GND
41	+5VDC	42	+5VDC
43	GND	44	NC

Table 3: IDE Interface

4.3 Serial Ports RS232 (CN8, CN9, CN10 and CN11)

The VSX104+ provides four PC-compatible asynchronous serial ports. All the serial ports can be enabled or disabled in through the BIOS setting, they can also be reconfigured to alternate I/O addresses and Interrupts.

RS232 Interface (CN8, CN9,CN10, CN11)			
TOP		BOTTOM	
Pin #	Signal	Pin #	Signal
1	DCD	2	DSR
3	RX	4	RTS
5	TX	6	CTS
7	DTR	8	RI
9	GND	10	FORCE C.R. ON

Table 4: RS232 Ports

4.4 Parallel Port (CN12)

The VSX104+ incorporates one IBM XT/AT compatible parallel port. It can be configured as bi-directional parallel port (SPP), enhanced parallel port (EPP) and extended capabilities parallel port (ECP) through the BIOS setting. The base address and the interrupts can also be configured or disabled.

Parallel Port (CN12)			
TOP		BOTTOM	
Pin #	Signal	Pin #	Signal
1	STRB-	2	AUTOFD-
3	PD0	4	ERR-
5	PD1	6	INIT-
7	PD2	8	SLCTIN-
9	PD3	10	GND
11	PD4	12	GND
13	PD5	14	GND
15	PD6	16	GND
17	PD7	18	GND
19	ACK-	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT	26	GND

Table 5: Parallel Port

4.5 Universal Serial Bus (CN13)

The VSX104+ provides two USB2.0 ports (USB0 and USB1). The USB 2.0 controller is a two-port host controller which contains one OHCI host controller and one EHCI host controller. Both ports support up to 127 devices at low-speed (1.5MHz), full-speed (12MHz) and high-speed (480MHz).

USB Interface (CN13)			
TOP		BOTTOM	
Pin #	Signal	Pin #	Signal
1	+5VDC	2	GND ISO
3	DATA-	4	GND
5	DATA+	6	DATA+
7	GND	8	DATA-
9	GND ISO	10	+5VDC

Table 6: USB Ports

4.6 MicroSD Socket (CN14)

The VSX104+ embeds a MicroSD socket interfaced to the internal USB2 port through a USB 2.0 card reader controller allowing the media to be detected as USB storage device.
The MicroSD can be used to boot an Operating System or as a storage device.

MicroSD Socket (CN14)			
Pin #	Signal	Pin #	Signal
1	DATA2	2	DATA3
3	CMD	4	VCC
5	CLK	6	GND
7	DATA0	8	DATA1

Table 7: MicroSD Interface

4.7 Redundancy Port (CN16)

The redundancy port of the VSX104+ provides the communication port and the control signals to interconnect two CPU boards together. It allows the CPU boards to exchange data and share buses and devices.

Redundancy Port (CN16)	
BOTTOM	
Pin #	**Signal**
1	GND
2	GPIO34
3	GPIO35
4	SYS-FAIL-OUT
5	MTBF-OUT
6	GPCS1
7	GPCS0
8	SYS-FAIL-IN
9	SYS-SW-IN
10	SYS-GPCS-IN
11	COM9 TX
12	COM9 RX
13	RESET / PWRGD

Table 8: Redundancy Port

4.8 PS/2-SPI Port (CN17)

The PS/2-SPI port of the VSX104+ provides connections for PS/2 Keyboard, PS/2 Mouse and external SPI devices.

PS/2-SPI Port (CN17)	
BOTTOM	
Pin #	**Signal**
1	SPI-DO
2	SPI-DI
3	SPI-CLK
4	SPI-CS
5	PS/2 MS DATA
6	PS/2 MS CLK
7	PS/2 KB DATA
8	PS/2 KB CLK
9	+5VDC
10	GND

Table 9: PS/2-SPI Port

4.9 JTAG Port (CN18)

This port can be used to re-program the BIOS when the internal flash is erased.

JTAG port (CN18)			
TOP		BOTTOM	
Pin #	Signal	Pin #	Signal
1	+3VDC	2	TCK
-	-	3	TDO
-	-	4	TDI
6	GND	5	TMS

Table 10: JTAG Port

4.10 PC/104 BUS (CN19 and CN21)

Both CN19 and CN21 provide the flexibility to attach PC/104 expansion modules to the VSX104+. These modules perform the functions of traditional ISA add-on cards in a PC environment. The bus also provides the main power input +5V.

PC/104 8-bit Connector (CN19)			
Pin #	**Signal**	**Pin #**	**Signal**
A1	/IOCHCK	B1	GND
A2	SD7	B2	RESETDRV
A3	SD6	B3	+5V
A4	SD5	B4	IRQ9
A5	SD4	B5	-5V
A6	SD3	B6	DRQ2
A7	SD2	B7	-12V
A8	SD1	B8	/0WS
A9	SD0	B9	+12V
A10	IOCHRDY	B10	GND(*)
A11	AEN	B11	/SMEMW
A12	SA19	B12	/SMEMR
A13	SA18	B13	/IOW
A14	SA17	B14	/IOR
A15	SA16	B15	/DACK3
A16	SA15	B16	DRQ3
A17	SA14	B17	/DACK1
A18	SA13	B18	DRQ1
A19	SA12	B19	/REFRESH
A20	SA11	B20	SYSCLK
A21	SA10	B21	IRQ7
A22	SA9	B22	N/A
A23	SA8	B23	IRQ5
A24	SA7	B24	IRQ4
A25	SA6	B25	IRQ3
A26	SA5	B26	/DACK2
A27	SA4	B27	TC
A28	SA3	B28	BALE
A29	SA2	B29	+5V
A30	SA1	B30	OSC
A31	SA0	B31	GND
A32	GND	B32	GND

Table 11: PC/104 8-bit Interface

PC/104 16-bit Connector (CN21)			
Pin #	**Signal**	**Pin #**	**Signal**
C0	GND	D0	GND
C1	/SBHE	D1	/MEMCS16
C2	LA23	D2	/IOCS16
C3	LA22	D3	IRQ10
C4	LA21	D4	IRQ11
C5	LA20	D5	IRQ12
C6	LA19	D6	IRQ15
C7	LA18	D7	IRQ14
C8	LA17	D8	/DACK0
C9	/MEMR	D9	DRQ0
C10	/MEMW	D10	/DACK5
C11	SD8	D11	DRQ5
C12	SD9	D12	/DACK6
C13	SD10	D13	DRQ6
C14	SD11	D14	/DACK7
C15	SD12	D15	DRQ7
C16	SD13	D16	+5V
C17	SD14	D17	/MASTER
C18	SD15	D18	GND
C19	GND(*)	D19	GND

Table 12: PC/104 16-bit Interface

4.11 PC/104+ BUS (CN20)

CN20 provides the flexibility to attach PCI-104 and/or PC/104+ expansion modules to the VSX104+. These modules perform the functions of traditional PCI add-on cards in a PC environment. The bus also provides the main power input +5V. The CPU board does not supply the +3.3V to the bus, it has to be generated externally to power the PC/104+ devices.

PC/104+ 32-bit Connector (CN20)				
Pin #	**A**	**B**	**C**	**D**
1	GND	NC	+5V	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	PMEX
7	AD14	AD13	GND	AD12
8	+3.3V	CBE1	AD15	+3.3V
9	SERR	GND	SB0	PAR
10	GND	PERR	+3.3V	SDONE
11	STOP	+3.3V	LOCK	GND
12	+3.3V	TRDY	GND	DEVSEL
13	FRAME	GND	IRDY	+3.3V
14	GND	AD16	+3.3V	C/BE2
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	N/A	GND	N/A	IDSEL2
19	AD24	C/BE3	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	N/A	GND	N/A	VI/O
24	GND	REQ2	+5V	N/A
25	N/A	VI/O	GNT2	GND
26	+5V	N/A	GND	N/A
27	CLK_PCI_2	+5V	CLK_PCI_3	GND
28	GND	INTD	+5V	RST
29	+12V	N/A	N/A	INTB
30	-12V	NC	NC	GND

Table 13: PC/104+ 32-bit Interface

4.12 LAN Interface 1 (CN22)

The VSX104+ is equipped with an Ethernet 10/100 BaseT. It provides 32 bit performance, PCI bus master capability and full compliance with IEEE 802.3u specifications. It supports 10Mbps and 100 Mbps N-way auto-negotiation operation and full duplex flow control compliant with IEEE 802.3x

LAN interface 1 (CN22)			
TOP		BOTTOM	
Pin #	Signal	Pin #	Signal
1	TX+	2	TX-
3	RX+	4	NC
5	NC	6	RX-
7	NC	8	NC

Table 14: LAN Interface 1

4.13 LAN Interface 2 (CN23)

The VSX104+ embeds an Intel 82551er Ethernet controller that provides an additional Ethernet 10/100 BaseT. It is interfaced through the 32 bit PCI bus and has bus master capability. It supports full duplex at 10Mbps and 100 Mbps and it has IEEE 802.3u auto-negotiation support. The flow control is compliant with IEEE 802.3x.

LAN interface 2 (CN23)			
TOP		BOTTOM	
Pin #	Signal	Pin #	Signal
1	TX+	2	TX-
3	RX+	4	NC
5	NC	6	RX-
7	NC	8	NC

Table 15: LAN Interface 2

4.14 Input Power (CN24)

The VSX104+ can be powered by supplying 5VDC and ground to CN24. Alternatively, the VSX104+ can be powered by supplying 5VDC through the PC104 connector (CN19 + CN21) with a PC104 power supply such as the Tri-M Engineering HE104 or HESC-104.

External Power (CN24)	
Pin #	**Signal**
1	+5VDC
2	GND

Table 16: Power connector

This is not a wide range input, a voltage exceeding +5VDC or a reverse polarity will cause damage to the board.

4.15 GPIO 0 Port (CN26)

The GPIO 0 port of the VSX104+ provides 8 input/output signals and a 5VDC supply to ease interfacing with external circuitry. The GPIO0 port can be configured through the BIOS settings or through I/O registers. Each bit can be programmed as input or output independently.

GPIO 0 Port (CN26)	
BOTTOM	
Pin #	**Signal**
1	GPIO0-bit0
2	GPIO0-bit1
3	GPIO0-bit2
4	GPIO0-bit3
5	GPIO0-bit4
6	GPIO0-bit5
7	GPIO0-bit6
8	GPIO0-bit7
9	+5VDC
10	GND

Table 17: GPIO 0 Port

CHAPTER 5: GENERAL PURPOSE INPUT/OUPUT

5.1 Overview

The VSX104+ provides many GPIO signals. Some are wired to the Redundancy connector (CN16) or the GPIO 0 port (CN26) and are free for personal use. Others are used to control some of the board settings. The direction register and the data register of both ports will have to be set to match the desired configuration. If all GPIO signals used for devices configuration are configured as input, the industry default setting will be applied.

5.2 GPIO Port 0

The GPIO port 0 bits 0 to 7 are wired to the GPIO 0 connector (CN26). They are free and can be used for personal use. As input these pins are pulled high with a 75KΩ pull-up and are 5 Volt tolerant. As output these pins can drive 8mA.

Direction register, Address: 0x98

Bit	7	6	5	4	3	2	1	0
Function	CN26 Pin8	CN26 Pin7	CN26 Pin6	CN26 Pin5	CN26 Pin4	CN26 Pin3	CN26 Pin2	CN26 Pin1

Table 18: GPIO 0 Direction Register

The Default value is 0x00 (all signals set as input), programming a bit to 1 change the configuration of the corresponding pin to output. This register can be configured through the BIOS settings.

These pins are directly connected to the processor, applying too much voltage or draining too much current could damage it.

Data register, Address: 0x78

Bit	7	6	5	4	3	2	1	0
Function	CN26 Pin8	CN26 Pin7	CN26 Pin6	CN26 Pin5	CN26 Pin4	CN26 Pin3	CN26 Pin2	CN26 Pin1

Table 19: GPIO 0 Data Register

When configured as input the bit will reflect the TTL level applied to the pin.
When configured as output a 0 set the pin to 0 Volt and a 1 set the pin to 3.3 Volt.

5.3 GPIO Port 1

The GPIO port 1 allows control of the RS232 transceiver of all the serial ports (COM1 to COM4). It also reports if a valid RS232 signal is applied to any of the serial ports.

Direction register, Address: 0x99

Bit	7	6	5	4	3	2	1	0
Function	COM4 Status	COM3 Status	COM2 Status	COM1 Status	COM4 PME	COM3 PME	COM2 PME	COM1 PME

Table 20: GPIO 1 Direction Register

The Default value is 0x00 (all signals set as input), all the serial ports have the power management disabled. Changing bits 0-3 to 1 allows control of the power management of the corresponding serial port through the data register.

Setting bits 4 TO 7 as output, could cause damage to the board because the signals will be in conflict with the transceiver output.

Data register, Address: 0x79

Bit	7	6	5	4	3	2	1	0
Function	COM4 Status	COM3 Status	COM2 Status	COM1 Status	COM3 PME	COM3 PME	COM2 PME	COM1 PME

Table 21: GPIO 1 Data Register

Status bit return 1 when a valid RS232 level is detected on the corresponding serial port.
PME bit set to 1 to force ON the transceiver of the corresponding serial port.
PME bit set to 0 to have the transceiver of the corresponding serial port to turning ON only when RS232 signal present.

5.4 GPIO Port 2

The GPIO port 2 allows control of the power switches of the USB ports (USB0 and USB1), ability to read the over current status of the USB ports (USB0 and USB1), select the Compact Flash socket to Master or Slave, and read/control the power management of the PCI devices.

Direction register, Address: 0x9A

Bit	7	6	5	4	3	2	1	0
Function	µSD WP	PCI PME	USB1 OVC	USB0 OVC	LEDs enable	CPF select	USB1 enable	USB0 enable

Table 22: GPIO 2 Direction Register

The Default value is 0x00 (all signals set as input), both USB ports (0 and 1) are enabled, the Compact Flash socket is configured as Master and the PCI power management is uncontrolled. Changing bits 0-1 to 1 allows control of the power switch of the corresponding USB port through the data register. Changing bit 2 to 1 allows to selection of the Compact Flash socket as Master or Slave through the data register. Changing bit 3 to 1 allows to turn ON/OFF the on-board LEDs through the data register. Changing the bit 6 to 1 will allow control of the PCI power management instead of monitoring it. Changing bit 7 to 1 allows to write protect the on-board Micro-SD through the data register.

Setting bits 4 and 5 as output could cause damage to the board because the signals will be in conflict with the USB switch output.

Data register, Address: 0x7A

Bit	7	6	5	4	3	2	1	0
Function	µSD WP	PCI PME	USB1 OVC	USB0 OVC	LEDs enable	CPF select	USB1 enable	USB0 enable

Table 23: GPIO 1 Data Register

USB enable return 1 when the power switch is turned ON and 0 when the switch is turned OFF.
USB OVC bit return 0 the USB device of the corresponding port is draining too much current.
PCI PME bit return 0 when the PCI power management is enable.
CPF select return 0 when Master and 1 when Slave.
LEDs enable return 1 when the on-board LEDs are turned OFF.
µSD WP return 1 when WRITE PROTECTED.

5.5 GPIO Port 3

The GPIO port 3 bit 0 to 3 are wired respectively to the PS/2-SPI connector (CN17) pin 2, 1, 3, 4 and bit 4 to 5 are wired respectively to the redundancy connector (CN16) pin 2 and 3 . When set as GPIO they are free and can be used for personal use. The bit 0 to 3 can also be configured as an external SPI port. As input these pins are pulled high with a 75KΩ pull-up and are 5 Volt tolerant. As output these pins can drive 8mA.

Direction register, Address: 0x9B

Bit	7	6	5	4	3	2	1	0
Function	C.R. FON	SPI SEL	CN16 Pin3	CN16 Pin2	CN17 Pin2	CN17 Pin1	CN17 Pin3	CN17 Pin4

Table 24: GPIO 3 Direction Register

The Default value is 0x00 (all signals set as input), programming a bit to 1 changes the configuration of the corresponding pin to output. When the GPIO port 3 is set as SPI port, bits 4 and 5 can still be used as GPIO. Changing the bit 6 to 1 allows to selection for the SPI port to be used internally or externally. Do not change the bit 7 to output, it will prevent the BIOS to work properly. All the configuration of the ports can be done through the BIOS settings.

These pins are directly connected to the processor, applying too much voltage or draining too much current could damage it.

Data register, Address: 0x7B

Bit	7	6	5	4	3	2	1	0
Function	C.R. detect	SPI SEL	CN16 Pin3	CN16 Pin2	CN17 Pin2	CN17 Pin1	CN17 Pin3	CN17 Pin4

Table 25: GPIO 3 Data Register

CN16/CN17: when configured as input the bit will reflect the TTL level applied to the pin.
CN16/CN17: when configured as output a 0 set the pin to 0 Volt and a 1 set the pin to 3.3 Volt.
SPI SEL: set to 0 to access the on board SPI flash, set to on to access external device.
C.R. Detect: return 0 when Console redirection forced ON, feature built into the BIOS.

GPIO port 3 bit 0 (CN17-Pin4) is shared with SPI-CS.
GPIO port 3 bit 1 (CN17-Pin3) is shared with SPI-CLK.
GPIO port 3 bit 2 (CN17-Pin1) is shared with SPI-DO.
GPIO port 3 bit 3 (CN17-Pin2) is shared with SPI-DI.

5.6 GPIO Port 4

The GPIO port 4 is shared with the RS232 port 1. All the signals are wired to an RS232 transceiver and therefore have limitations as GPIO. We strongly suggest to keep this port configured as Serial port 1 to avoid any mis-configuration that could cause damage to the board.

Direction register, Address: 0x9C

Bit	7	6	5	4	3	2	1	0
Function	Input only	Input only	Output only	Input only	Input only	Output only	Output only	Input only

Table 26: GPIO 4 Direction Register

The Default value is 0x00 (all signals set as input), programming a bit to 1 change the configuration of the corresponding pin to output. All the configuration of the port can be done through the BIOS settings.

Any mis-configuration of the GPIO port 4 registers can damage the processor and/or the RS232 transceiver.

Data register, Address: 0x7C

Bit	7	6	5	4	3	2	1	0
Function	CN8 Pin6	CN8 Pin2	CN8 Pin7	CN8 Pin3	CN8 Pin8	CN8 Pin4	CN8 Pin5	CN8 Pin1

Table 27: GPIO 4 Data Register

The inputs will reflect the RS232 level applied to the pin.
The outputs will drive an RS232 level to the pin (-6V, 6V).

GPIO port 4 bit 0 (CN8-Pin1) is shared with Serial port 1 DCD.
GPIO port 4 bit 1 (CN8-Pin5) is shared with Serial port 1 TX.
GPIO port 4 bit 2 (CN8-Pin4) is shared with Serial port 1 RTS.
GPIO port 4 bit 3 (CN8-Pin8) is shared with Serial port 1 RI.
GPIO port 4 bit 4 (CN8-Pin3) is shared with Serial port 1 RX.
GPIO port 4 bit 5 (CN8-Pin7) is shared with Serial port 1 DTR.
GPIO port 4 bit 6 (CN8-Pin2) is shared with Serial port 1 DSR.
GPIO port 4 bit 7 (CN8-Pin6) is shared with Serial port 1 CTS.

CHAPTER 6: WATCHDOG TIMER

6.1 Overview

A watchdog is a device providing a system with a way to recover when the software is not responding. The circuitry is composed of a 24 bits counter incrementing at a rate of 32.768KHz and is supposed to be continuously cleared by the running software. When the software is not responding, the counter is not cleared and when it reaches a pre-programmed value, the circuitry will generate an interrupt or a system reset. The Vortex86SX embeds two watchdog timers.

6.2 WDT0 Registers

The WDT0 registers can be accessed through the index port 0x22 and the data port 0x23.
These registers are used to configure the time out, to select the event generated and to clear the counter. The time out can be programmed from 30.5 µsec to 512 sec with a resolution of 30.5 µsec.
The configuration of the watchdog 0 can be performed in the BIOS settings.

Index: 0x37

Bit	7	6	5	4	3	2	1	0
Function	X	EN	X	X	X	X	X	X

Table 28: WDT0 Enable Register

EN: set to 1 to enable the WDT0

Index: 0x38

Bit	7	6	5	4	3	2	1	0
Function	EVN3	EVN2	EVN1	EVN0	X	X	X	X

Table 29: WDT0 Event Register

EVN[3-0]	Signal	EVN[3-0]	Signal	EVN[3-0]	Signal	EVN[3-0]	Signal	EVN[3-0]	Signal
0001	IRQ3	0100	IRQ6	0111	IRQ10	1010	IRQ14	1101	RESET
0010	IRQ4	0101	IRQ7	1000	IRQ11	1011	IRQ15	0001	Rsvd
0011	IRQ5	0110	IRQ9	1001	IRQ12	1100	INMI	0001	Rsvd

Index: 0x39

Bit	7	6	5	4	3	2	1	0
Function	D7	D6	D5	D4	D3	D2	D1	D0

Table 30: WDT0 Counter Low

Index: 0x3A

Bit	7	6	5	4	3	2	1	0
Function	D15	D14	D13	D12	D11	D10	D9	D8

Table 31: WDT0 Counter Mid

Index: 0x3B

Bit	7	6	5	4	3	2	1	0
Function	D23	D22	D21	D20	D19	D18	D17	D16

Table 32: WDT0 Counter High

D[23-0]: WDT0 24 bits counter.

Index: 0x3C

Bit	7	6	5	4	3	2	1	0
Function	TO	CLR	X	X	X	X	X	X

Table 33: WDT0 Clear Register

CLR: Write 1 reset the watchdog timer.
TO: read only bit, set to 1 when the watchdog time out occurred.

6.3 WDT1 Registers

The WDT1 registers can be accessed through the I/O ports 0x68 to 0x6D.
These registers are used to configure the time out, to select the event generated and to clear the counter. The time out can be programmed from 30.5 µsec to 512 sec with a resolution of 30.5 µsec.
The configuration of the watchdog 1 can be performed in the BIOS settings.

Address: 0x68

Bit	7	6	5	4	3	2	1	0
Function	X	EN	X	X	X	X	X	X

Table 34: WDT1 Enable Register

EN: set to 1 to enable the WDT1

Address: 0x69

Bit	7	6	5	4	3	2	1	0
Function	EVN3	EVN2	EVN1	EVN0	X	X	X	X

Table 35: WDT1 Event Register

EVN[3-0]	Signal	EVN[3-0]	Signal	EVN[3-0]	Signal	EVN[3-0]	Signal	EVN[3-0]	Signal
0001	IRQ3	0100	IRQ6	0111	IRQ10	1010	IRQ14	1101	RESET
0010	IRQ4	0101	IRQ7	1000	IRQ11	1011	IRQ15	0001	Rsvd
0011	IRQ5	0110	IRQ9	1001	IRQ12	1100	INMI	0001	Rsvd

Address: 0x6A

Bit	7	6	5	4	3	2	1	0
Function	D7	D6	D5	D4	D3	D2	D1	D0

Table 36: WDT1 Counter Low

Address: 0x6B

Bit	7	6	5	4	3	2	1	0
Function	D15	D14	D13	D12	D11	D10	D9	D8

Table 37: WDT1 Counter Mid

Address: 0x6C

Bit	7	6	5	4	3	2	1	0
Function	D23	D22	D21	D20	D19	D18	D17	D16

Table 38: WDT1 Counter High

D[23-0]: WDT1 24 bits counter.

Address: 0x6D

Bit	7	6	5	4	3	2	1	0
Function	TO	CLR	X	X	X	X	X	X

Table 39: WDT1 Clear Register

CLR: Write 1 reset the watchdog timer.
TO: read only bit, set to 1 when the watchdog time out occurred.

CHAPTER 7: CMOS RAM

7.1 Overview

The CMOS RAM is a 128 bytes memory part of the RTC circuitry powered by the battery.
This memory is usually used by the system to store the BIOS settings, the date and time.
The Vortex86SX has 20 bytes of this memory reserved for customization.
These 20 bytes are free for use and are not part of the checksum calculation.

7.2 CMOS RAM mapping

The CMOS RAM can be accessed through the index port 0x70 and the data port 0x71.

Index 0x70	Data 0x71
0x00 ~ 0x4B	BIOS Settings
0x4C ~ 0x5F	Free Space
0x60 ~ 0x7F	BIOS Settings

Table 40: CMOS RAM mapping

Index 0x00 to 0x4B and 0x60 to 0x7F are used by the system, any change in this area may cause the system to crash or work abnormally.

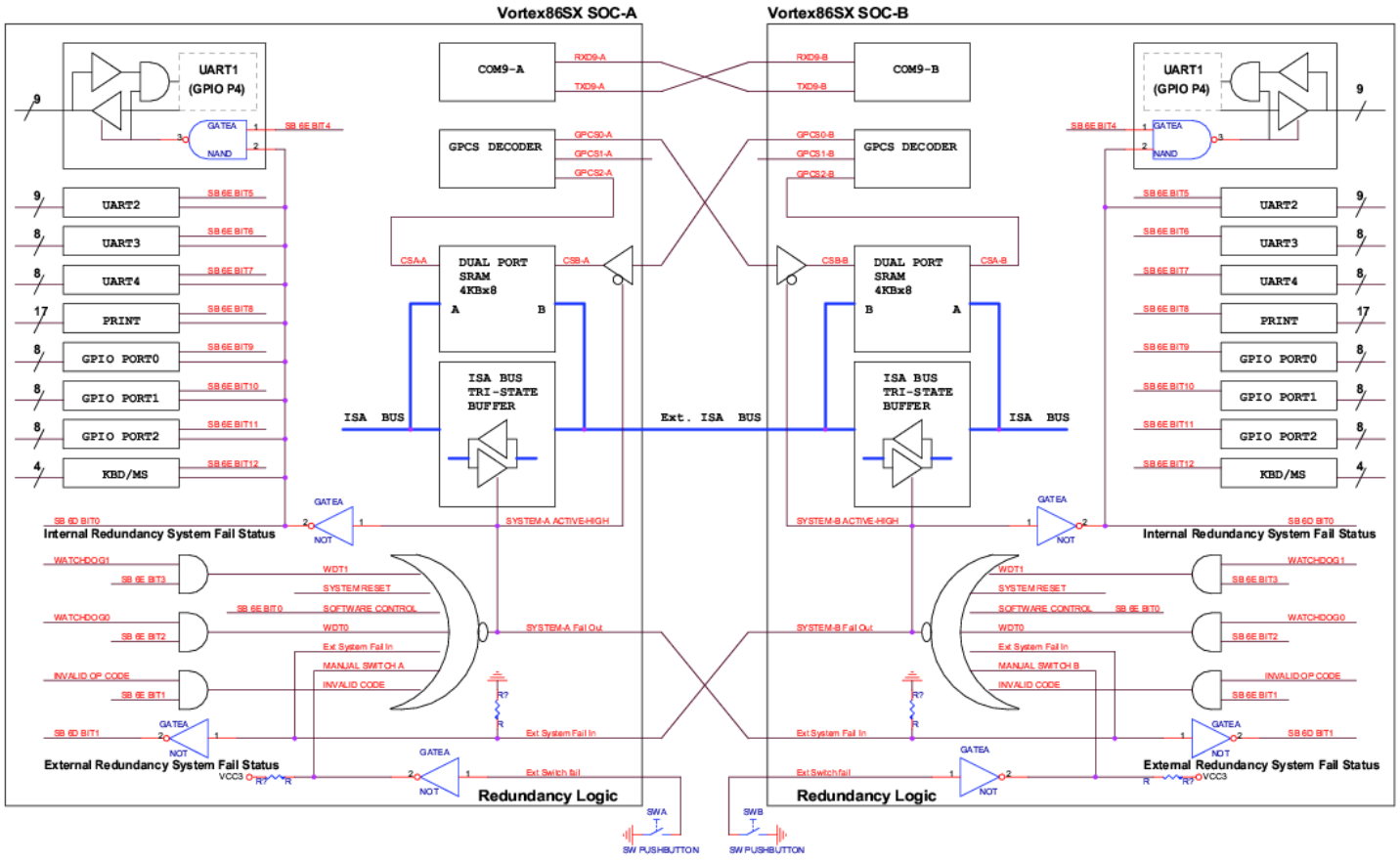
CHAPTER 8: REDUNDANCY

8.1 Overview

The Vortex86SX embeds some additional circuitry allowing two system boards to be connected together for redundancy purposes. This circuitry is composed of additional tri-state buffers allowing some buses and devices to be interconnected, extra logic to control these buffers and the systems status and communication channels to exchange information between both systems.

8.2 Block diagram

The following diagram shows how the system CPU can be interconnected.
The logic and communication ports are interconnected to signal the other CPU when a fail state occurs and to keep the data up to date on both CPUs.



Vortex86SX Redundancy System Block Diagram

8.3 Tri-stated Devices

To allow two CPUs to control the same devices, an isolation circuitry has to be put in place to avoid any conflict that cause damage to the system. The Vortex86SX has several ports protected with tri-state buffers. These ports are the four UARTs, the parallel port, the GPIO ports 0 to 2, the PS/2 interface and the entire PC/104 bus. Additionally the VSX104+ will turn off automatically all the RS232 transceivers when the output fail signal is set.

8.4 System intercommunication

For a redundant system to work both CPUs need to know what is the global status of the system, the spare CPU needs to know what the running CPU is doing at any moment. To do so both CPUs need to exchange data. The Vortex86SX has two communication ports dedicated to the redundancy port, one serial port and one dual port SRAM accessible through the PC104 bus outside the tri-state buffer. This SRAM can be accessed internally and externally to allow data exchange between both CPUs.

CHAPTER 9: ONBOARD SPI FLASH

9.1 Overview

The VSX104+ version 3 embeds a 2MBytes SPI flash supported by the BIOS as floppy drive.
The BIOS performs a floppy emulation over the SPI allowing an OS relying on the BIOS like DOS to access it as if it was a real floppy. OS not relying on the BIOS like Linux will need a driver to support the feature. The size of the flash is entirely accessible, it is not limited to 1.44MB.
This feature can be enabled through the BIOS settings (see Chapter 12: BIOS).

9.2 SPItool

When enabled in the BIOS, the SPI flash should be directly accessible in DOS.
However, not every version of DOS is able to always format it properly.
As a workaround DMP provides a tool called "spitool.exe" allowing you to format it properly under any version of DOS. This tool is also able to erase the flash, save the content of the SPI flash to a file and re-load an SPI flash from a file image.

SPITOOL FORMAT

Initialize the SPI flash and format it using FAT.

SPITOOL ERASE

Erase the entire content of the SPI flash, the flash will content only 0xFF.

SPITOOL READ FILENAME

Read entire the content of the SPI flash and save into a file.

SPITOOL WRITE FILENAME

Write the content of a file into the SPI flash.

CHAPTER 10: ONBOARD LED's

10.1 Overview

The VSX104 version 3 embeds three bi-color LED's displaying system status and devices activities. The LED's can be disabled to reduce the power consumption of the board (see Chapter 12: BIOS).

10.2 LED1

The LED1 a bi-color GREEN-RED and it is use to display the status of the PWRGOOD signal and the activity of the IDE controller.
The LED is steady green when all the on-board power are good (V_{core}, 1.8V and 3.3V) and the master reset is released (PWRGOOD signal inserted).
The LED is steady green and flashing red when the IDE interface is accessed, Hard-drive and/or Compact Flash.

10.3 LED2

The LED2 is bi-color BLUE-RED and it is use to display the status of the on-board Micro-SD interface.
The LED is steady red when there is no Micro-SD inserted into the slot.
The LED is steady blue when there is a Micro-SD inserted into the slot.
The LED is steady blue and flashing red when Micro-SD is accessed, in reading or writing.

10.4 LED3

The LED3 is bi-color GREEN-YELLOW and it is use to display the status of the first on-board Ethernet controller (built-in Ethernet controller of the Vortex86SX CPU).
The LED is steady green when there is network link.
The LED is steady green and flashing yellow when there is network activities.

10.5 LED4

The LED4 is bi-color GREEN-YELLOW and it is use to display the status of the second on-board Ethernet controller (on-board Intel Ethernet controller 82551IT).
The LED is steady green when there is network link.
The LED is steady green and flashing yellow when there is network activities.

CHAPTER 11: CONSOLE REDIRECTION

11.1 Overview

When the VSX104 is not equipped with video card, the display can be redirected to one of the serial port. The console redirection can be enabled and configured through the BIOS settings (see Chapter 12: BIOS). In addition when the console redirection is disabled in the BIOS settings and no video card are available, the console redirection can be forced ON by connecting the pin#10 of one of the serial ports to ground (see Chapter 4: CONNECTORS).

11.2 Force Console Redirection ON

Even when disabled in the BIOS settings, the console redirection can be forced ON using a console redirection cable or by connecting pin#10 of any serial port to ground.
The console won't automatically be enabled to the selected serial port but will follow the BIOS settings.
As example: if the pin#10 of COM4 is grounded but the console redirection is configured to COM1 in the BIOS settings, the console redirection will be assigned to COM1.

11.3 Default settings

Remote Access: Disabled (will be override when pin#10 grounded).
Serial port number: COM1.
Base Address, IRQ: 3F8h, 4.
Serial Port Mode: 115200 8,N,1.
Flow Control: none.
Redirection after POST: Always.
Terminal type: ANSI.
VT-UTF8 Combo Key: Enabled.
Sredir Memory Display Delay: No Delay.

Any change applied to the console redirection configuration will be used when forcing it ON.

CHAPTER 12: BIOS

12.1 Main menu

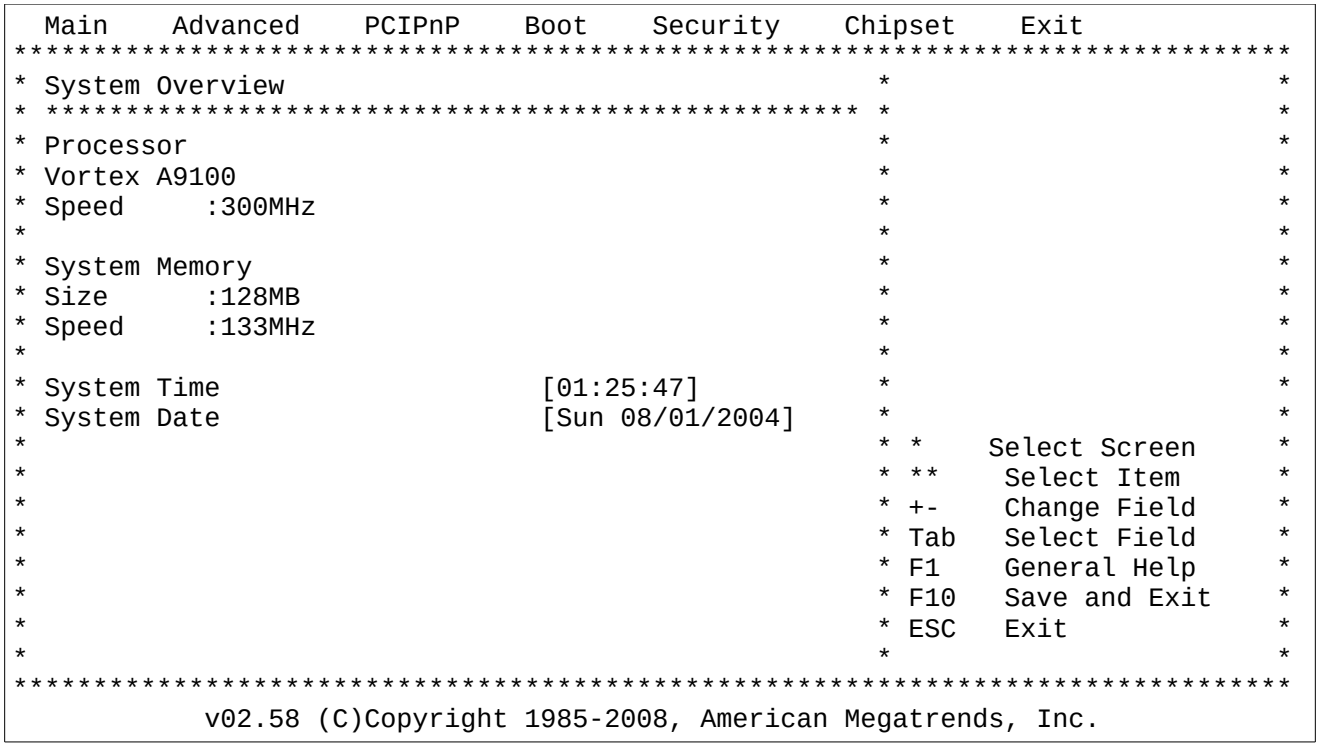


Figure 2: Main menu.

The Main page provides the system overview:

- The CPU model and speed.
- The memory size and bus speed.
- The time setting of the RTC.
- The date setting of the RTC.

12.2 Advanced Settings

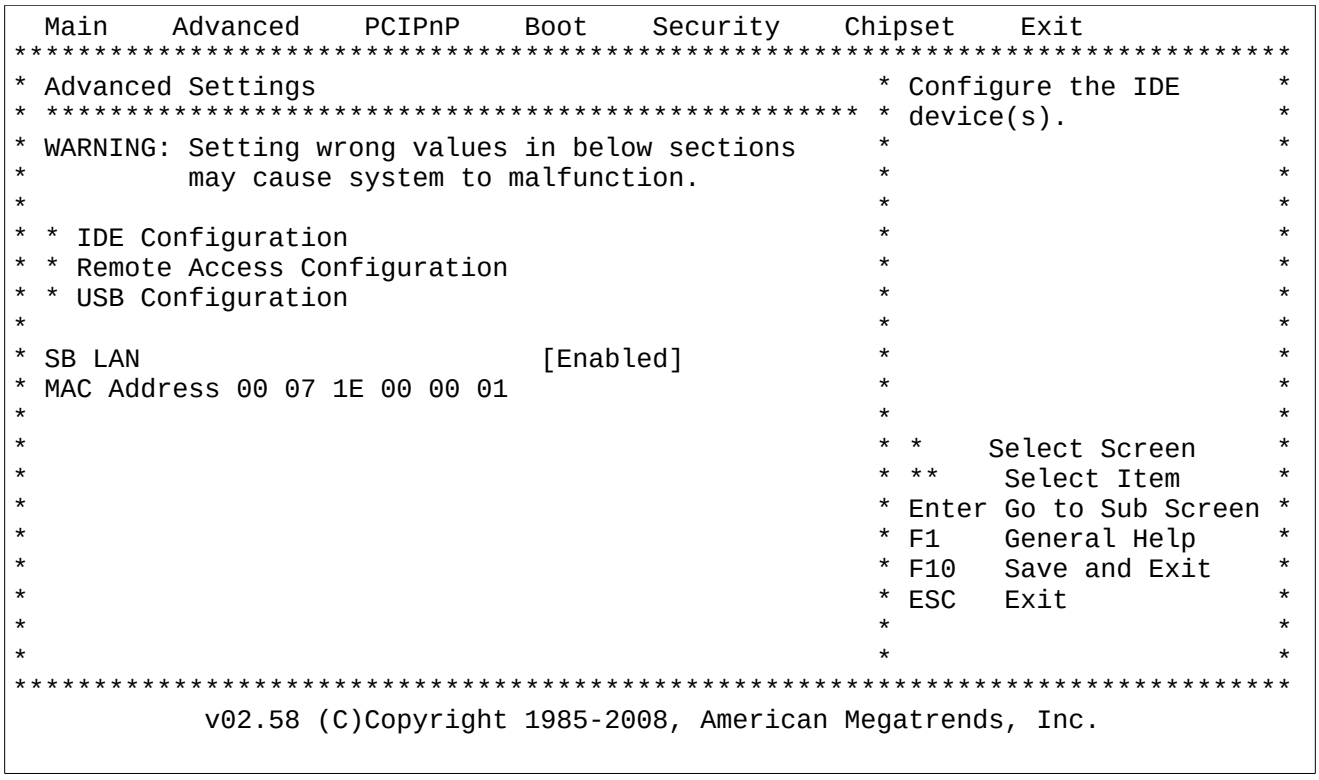


Figure 3: Advanced Settings.

The Advanced page provides:

- The IDE configuration sub-menu.
- The Console Redirection configuration sub-menu.
- The USB configuration sub-menu.
- The enable/disable of the LAN.
- The display of the MAC address.

12.3 IDE Controller Configuration

```
          Advanced
*************************************************************************
* IDE Configuration                                  * While entering setup,  *
* ************************************************ * BIOS auto detects the  *
* OnBoard PCI IDE Controller     [Primary]           * presence of IDE        *
*                                                    * devices. This displays *
* * Primary IDE Master              : [Hard Disk]    * the status of auto     *
* * Primary IDE Slave               : [Not Detected] * detection of IDE       *
* * Secondary IDE Master            : [Not Detected] * devices.               *
* * Secondary IDE Slave             : [Not Detected] *                        *
*                                                    *                        *
* Hard Disk Write Protect        [Disabled]          *                        *
* IDE Detect Time Out (Sec)      [35]                *                        *
* ATA(PI) 80Pin Cable Detection  [Host & Device]     *                        *
* Hard Disk Delay                [2 Second]          * *    Select Screen     *
* OnBoard IDE Operate Mode       [Legacy Mode]       * **    Select Item      *
* Not Program PIO mode           [Disabled]          * Enter Go to Sub Screen *
*                                                    * F1    General Help     *
*                                                    * F10   Save and Exit    *
*                                                    * ESC   Exit             *
*                                                    *                        *
*                                                    *                        *
*************************************************************************
           v02.58 (C)Copyright 1985-2008, American Megatrends, Inc.
```

Figure 4: IDE Controller Configuration.

On-Board PCI IDE Controller has to be set to PRIMARY only, the secondary is not available on this board. Primary IDE Master/Slave is auto-detected but can also be set manually through the sub-menu. Secondary IDE Master/Slave is unused.

Hard Disk Write Protect: will deny any write to the device when enabled.
IDE Detect Time Out: set the maximum time in sec. the BIOS will try to auto-detect the connected device.
ATA(PI) 80Pin Cable Detection: will allow high speed DMA transfer when 80 pins cable connected.
Hard Disk Delay: set the time the BIOS will wait for a device to be ready.
OnBoard IDE Operate mode: set the I/O and memory addresses of the IDE interface. Legacy uses the standard addresses of an IDE controller when Native will use the 8212 controller native addresses.
Not Program PIO mode: gives indication to the controller where are the devices when they can not be detected.

12.4 IDE Devices Configuration

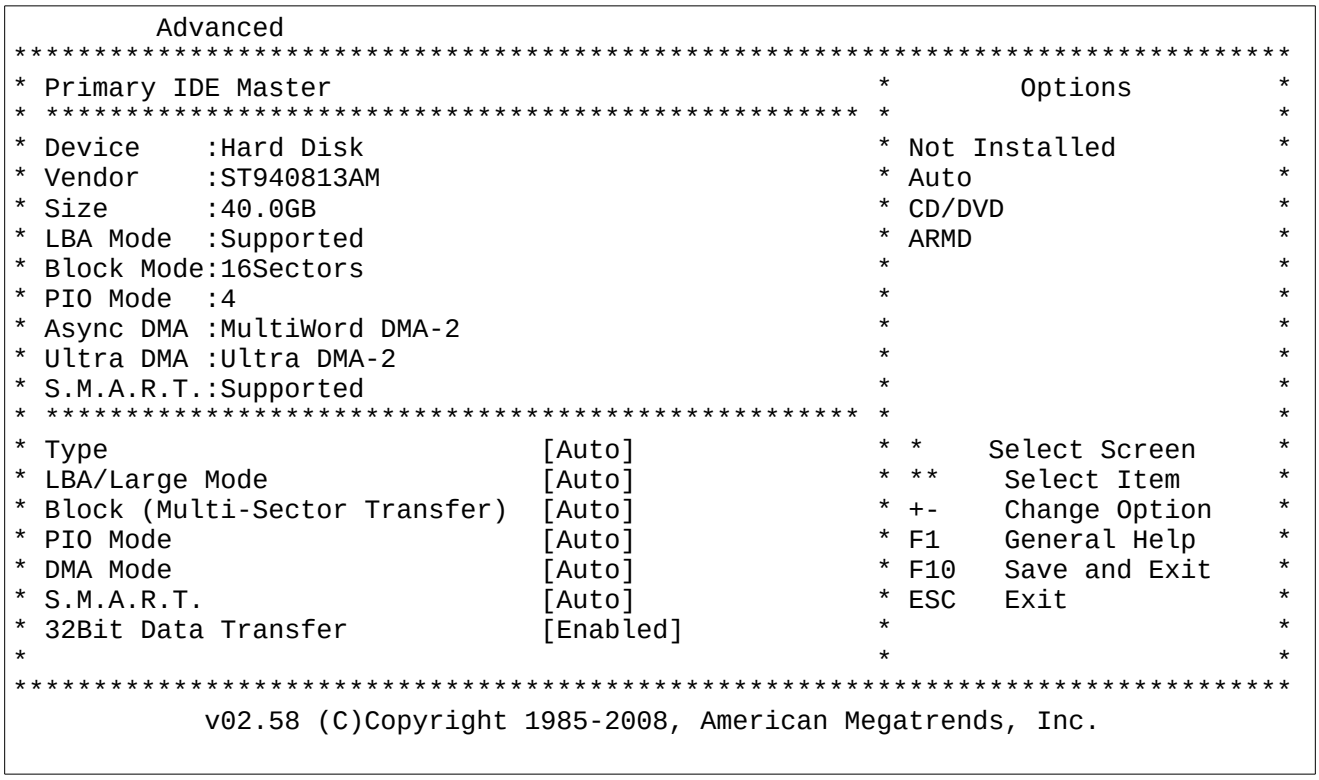


Figure 5: IDE Devices Configuration.

This page displays the specifications of the detected IDE device.
Available options will be automatically enable when set on Auto.
They can also be manually enabled or disabled.

Type: select the type of the device, removable, CDROM, auto or not installed.
Mode: LBA or Large.
Block: enable or disable the multiple sector transfer.
PIO Mode: force the PIO mode from 0 to 4 or use the detected mode.
DMA Mode: auto only.
S.M.A.R.T.: enable/disable Smart Monitoring, Analysis and Reporting Technology.
32bit Data Transfer: enable/ disable 32bit data transfer.

12.5 Console Redirection Configuration

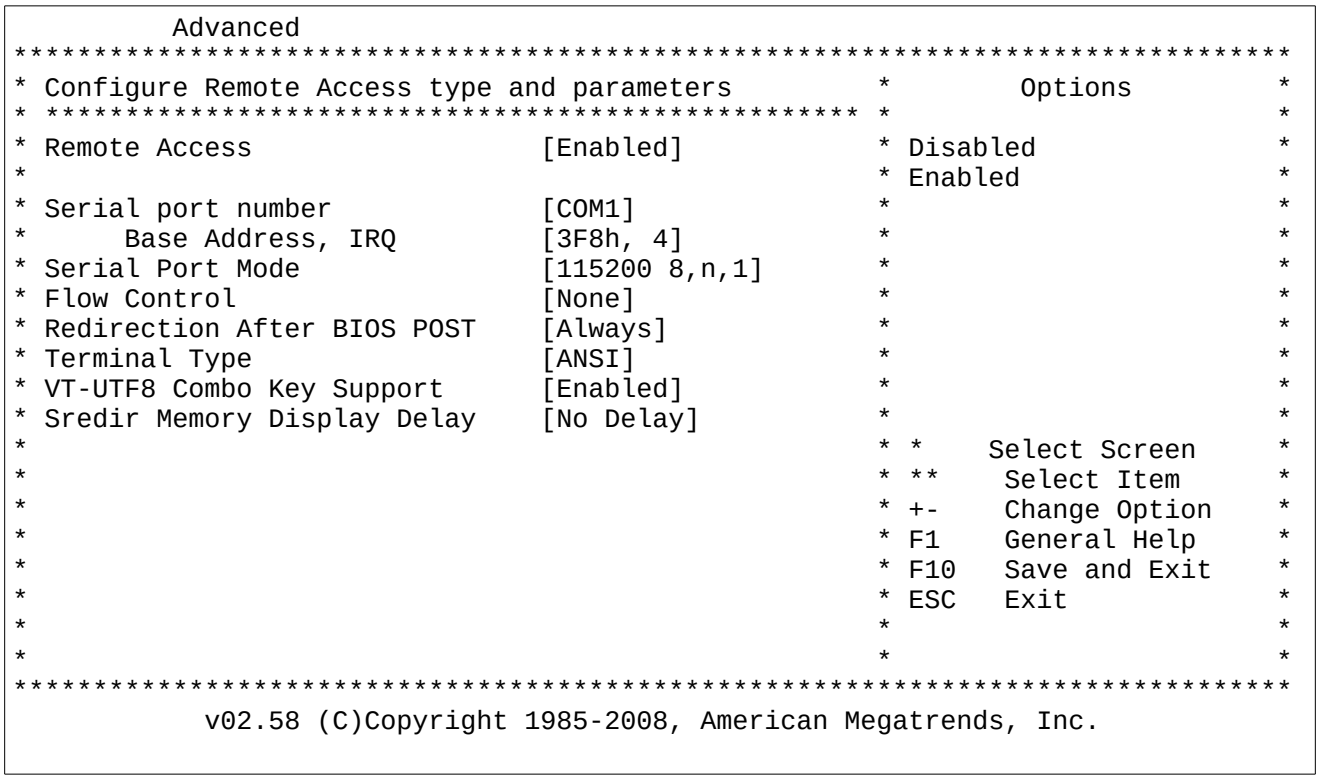


Figure 6: Console Redirection Configuration.

Console redirection options when feature activated.

Remote Access: enable/disable the console redirection.
Serial port number: select the physical serial port.
Base Address, IRQ: assign the base address and IRQ of the selected port.
Serial Port Mode: select communication speed and protocol.
Flow Control: set the flow control to hardware, software or none.
Redirection after POST: select if the console redirection is always enable, only during Initialization or during initialization and boot loader.
Terminal type: select the terminal emulation.
VT-UTF8 Combo Key: allows to use VT-UTF8 combo key also on ANSI and VT100 terminal.
Sredir Memory Display Delay: delay between display memory and console redirection refresh.

12.6 USB Controller Configuration

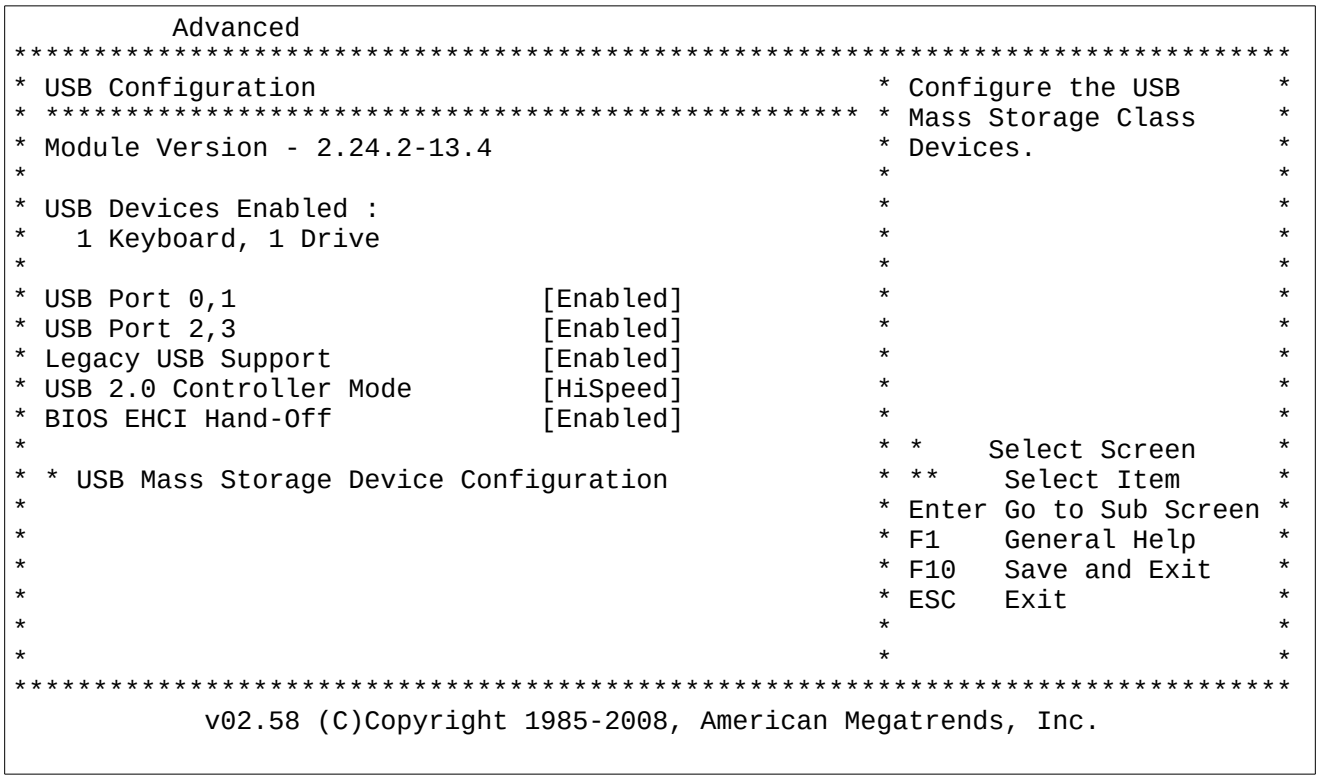


Figure 7: USB Controller Configuration.

This page displays the USB devices detected by the BIOS, configures the USB features supported by the BIOS and enable/disable the USB controllers.

USB Port 0,1: enable/disable the external USB ports available on the connector CN13.
USB Port 2,3: enable/disable the onboard microSD controller.
Legacy USB Support: allows the BIOS to handle USB keyboard and mouse when enable.
USB 2.0 Controller Mode: allows to use the USB 2.0 controller in high speed or full speed.
BIOS EHCI hand-off: enable/disable support for EHCI hand-off feature.

12.7 USB Storage Devices Configuration

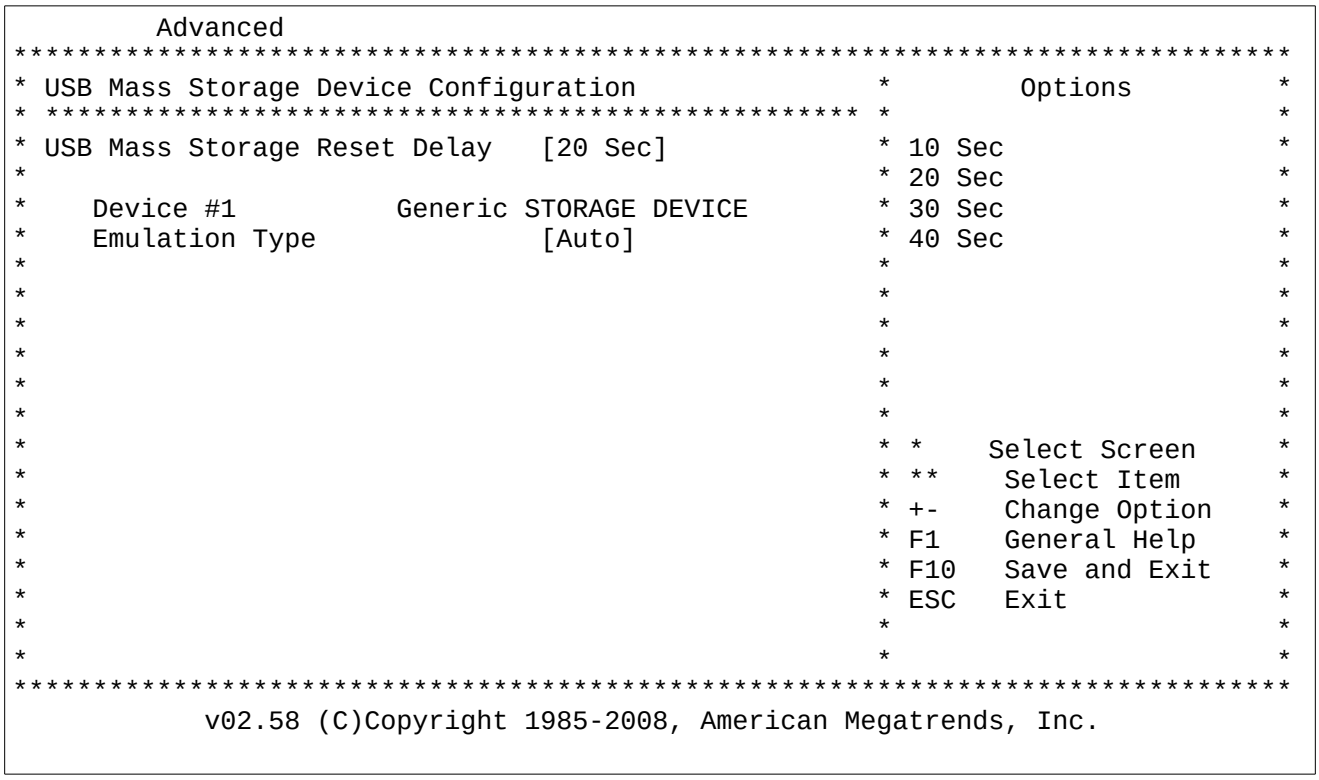


Figure 8: USB Storage Devices Configuration.

This menu shows the USB storage devices detected by the BIOS and allows selection of which emulation mode they will be used (floppy, hard-drive, cdrom).

12.8 PCI/PNP Configuration

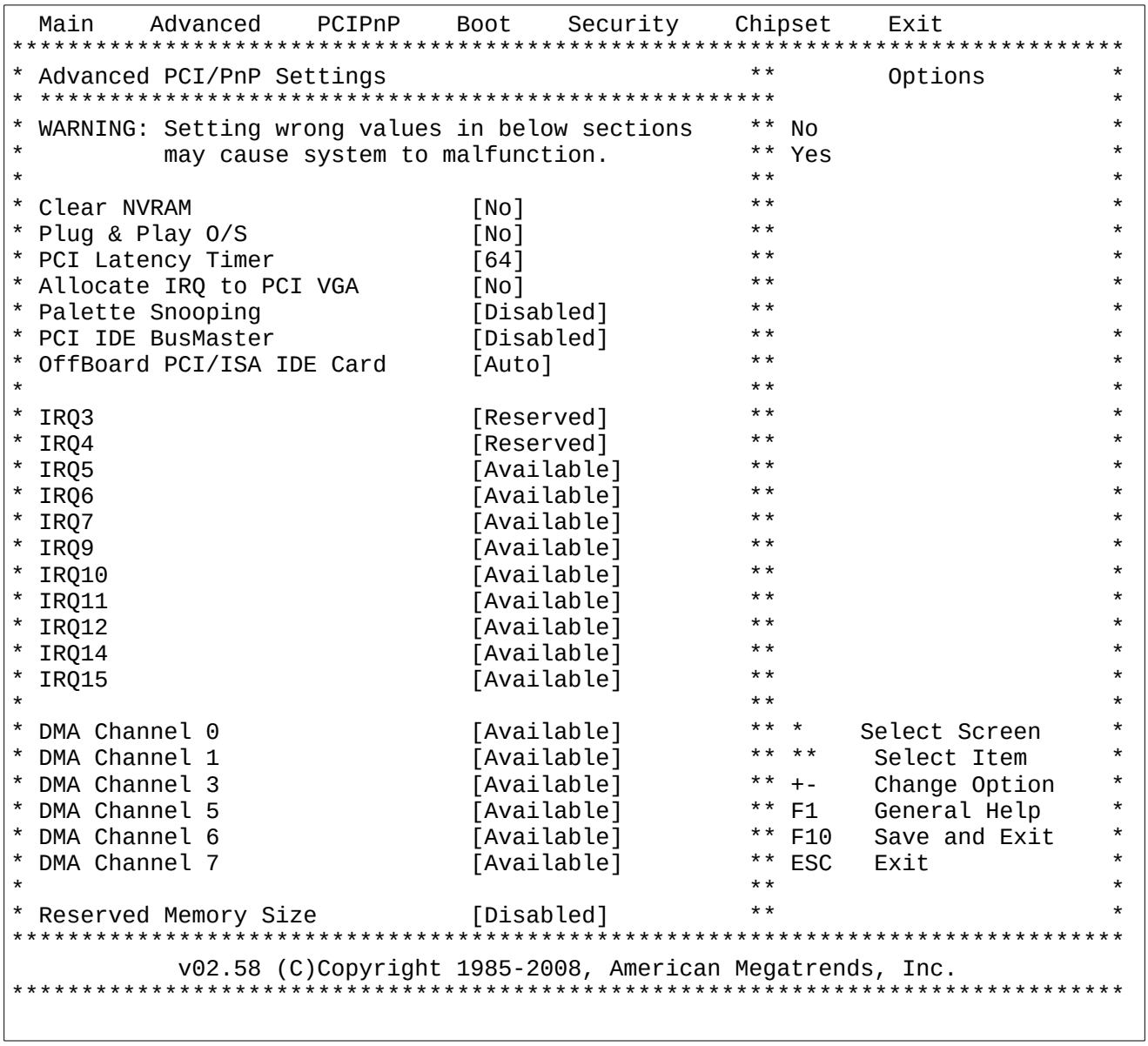


Figure 9: PCI/PNP Configuration.

PCI / Plug and Play configuration sub menu. It allows to reserve some of the system resources to avoid devices conflict.

Clear NVRAM: clear the NVRAM during the system boot.
Plug & Play O/S: allow the OS to modify the settings for P&P operation.
PCI Latency Timer: set the PCI device latency in number of PCI clocks.

Allocate IRQ to PCI VGA: allow or restrict the system from providing an IRQ for the VGA.
Palette Snooping: allows old PCI capturing card the use the VGA color palette.
PCI IDE BUSMaster: allow/prevent the IDE to be PCI bus master.
Offboard PCI/ISA IDE card: specify the location of an additional off board IDE controller or let the system auto-detect if any present.

IRQ3: reserve the IRQ3 for a legacy ISA device or make it available for PCI/PnP use.
IRQ4: reserve the IRQ4 for a legacy ISA device or make it available for PCI/PnP use.
IRQ5: reserve the IRQ5 for a legacy ISA device or make it available for PCI/PnP use.
IRQ6: reserve the IRQ6 for a legacy ISA device or make it available for PCI/PnP use.
IRQ7: reserve the IRQ7 for a legacy ISA device or make it available for PCI/PnP use.
IRQ9: reserve the IRQ9 for a legacy ISA device or make it available for PCI/PnP use.
IRQ10: reserve the IRQ10 for a legacy ISA device or make it available for PCI/PnP use.
IRQ11: reserve the IRQ11 for a legacy ISA device or make it available for PCI/PnP use.
IRQ12: reserve the IRQ12 for a legacy ISA device or make it available for PCI/PnP use.
IRQ14: reserve the IRQ14 for a legacy ISA device or make it available for PCI/PnP use.
IRQ15: reserve the IRQ15 for a legacy ISA device or make it available for PCI/PnP use.

DMA Channel 0: reserve the DMA0 for a legacy ISA device or make it available for PCI/PnP use.
DMA Channel 1: reserve the DMA1 for a legacy ISA device or make it available for PCI/PnP use.
DMA Channel 3: reserve the DMA3 for a legacy ISA device or make it available for PCI/PnP use.
DMA Channel 5: reserve the DMA5 for a legacy ISA device or make it available for PCI/PnP use.
DMA Channel 6: reserve the DMA6 for a legacy ISA device or make it available for PCI/PnP use.
DMA Channel 7: reserve the DMA7 for a legacy ISA device or make it available for PCI/PnP use.

Reserved Memory Size: disable or set the memory size used by ISA devices.

12.9 Boot menu

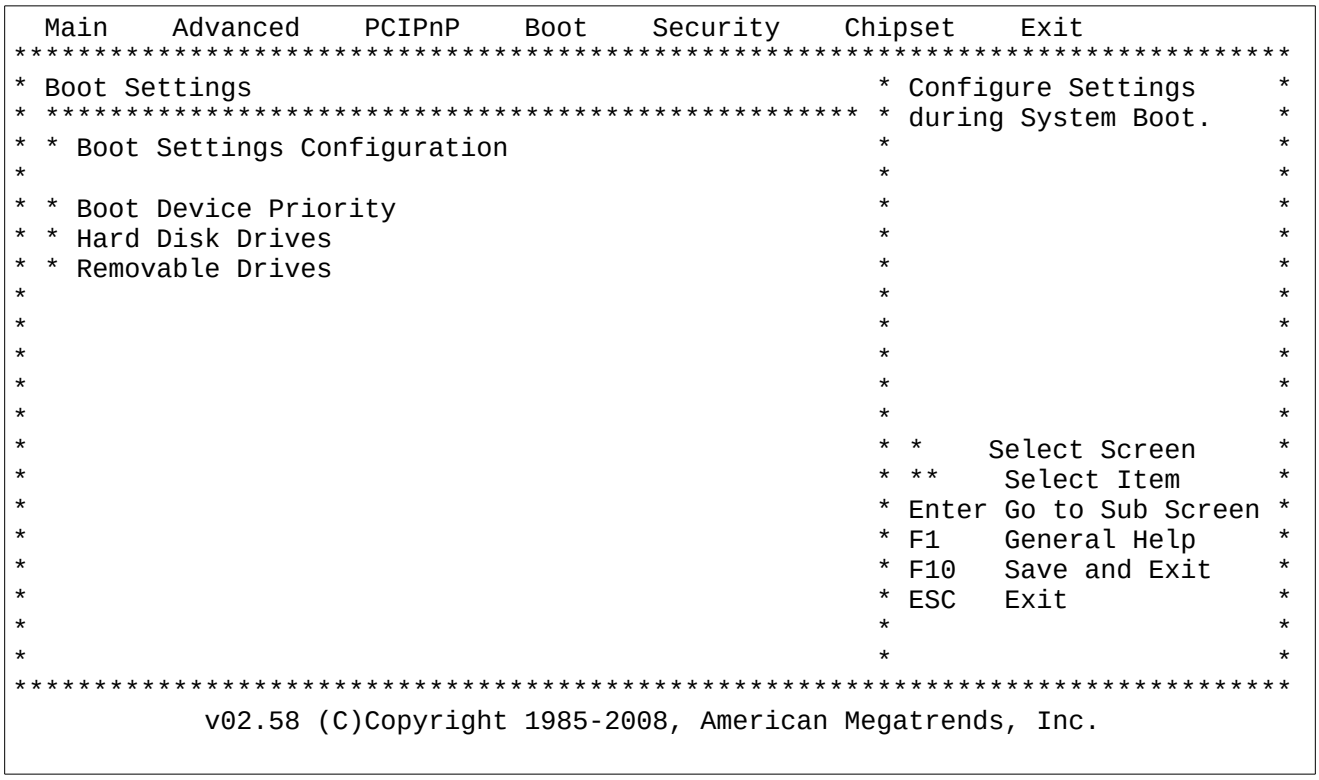


Figure 10: Boot menu.

The Boot settings page provides:

- Access to the Boot configuration option page.
- Setting of the boot priority of the detected devices for each category.
- Select of the boot priority of each category.

12.10 Boot Options

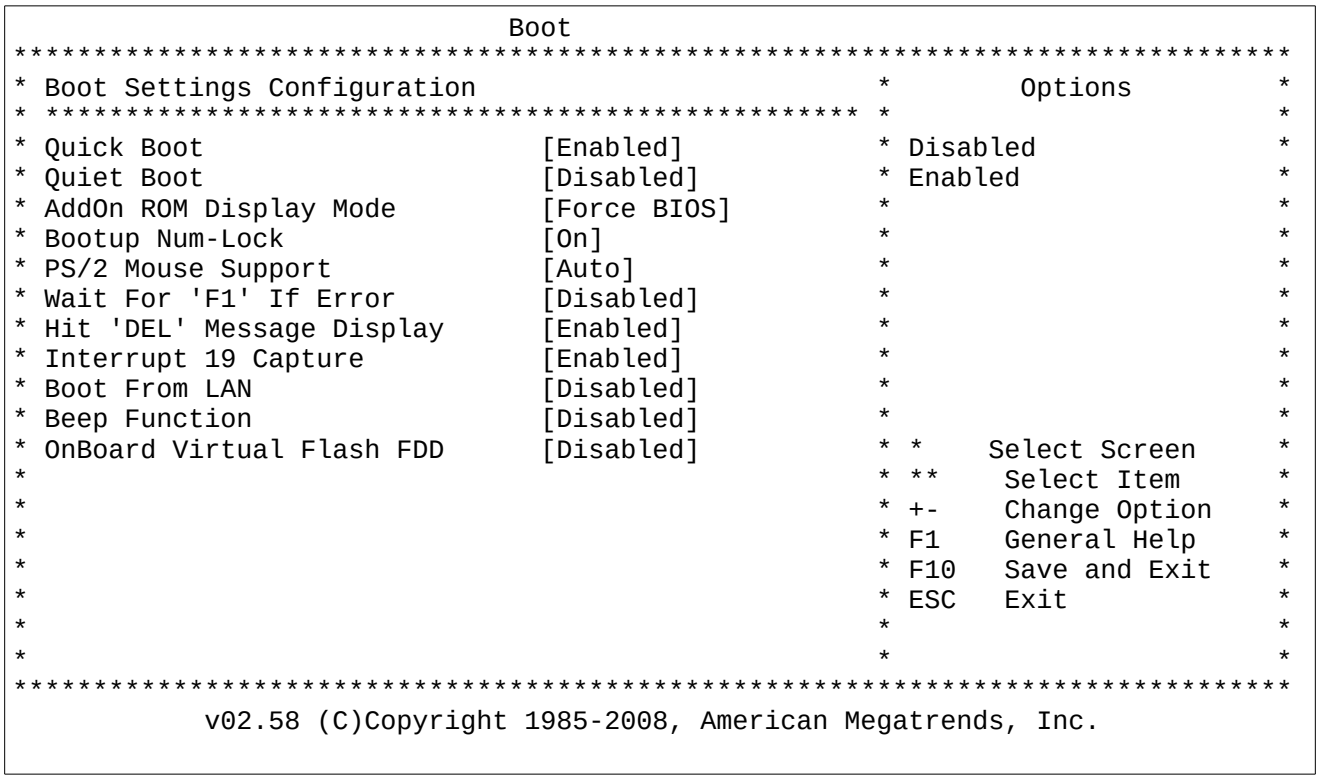


Figure 11: Boot Options.

This page allows to configure the startup options.

Quick Boot: allow to skip some Power On Self Test (POST) to reduce the boot time.
Quiet Boot: allow to display the POST messages or the OEM logo.
AddOn Rom Display Mode: force a third party BIOS to display during system boot.
Bootup Num-Lock: set the the numeric keypad to numeric during the boot up when ON.
PS/2 Mouse Support: prevents the PS/2 mouse from using the system resources when disabled.
Wait For 'F1' If Error: prevent/allow the system to stop when error detected by the BIOS.
Hit 'DEL' Message Display: show/hide the message "Hit Del to enter Setup" during boot.
Interrupt 19 Capture: prevent/allow option ROM such as network controllers to trap INT19.
Boot from LAN: prevent/ select the LAN boot function.
Beep Function: enable/disable the system to generate beep during the boot.
when set the system will generate one beep by USB device detected.
OnBoard Virtual Flash FDD: allow to emulate a floppy drive using an SPI flash.

12.11 Boot Priority Overall

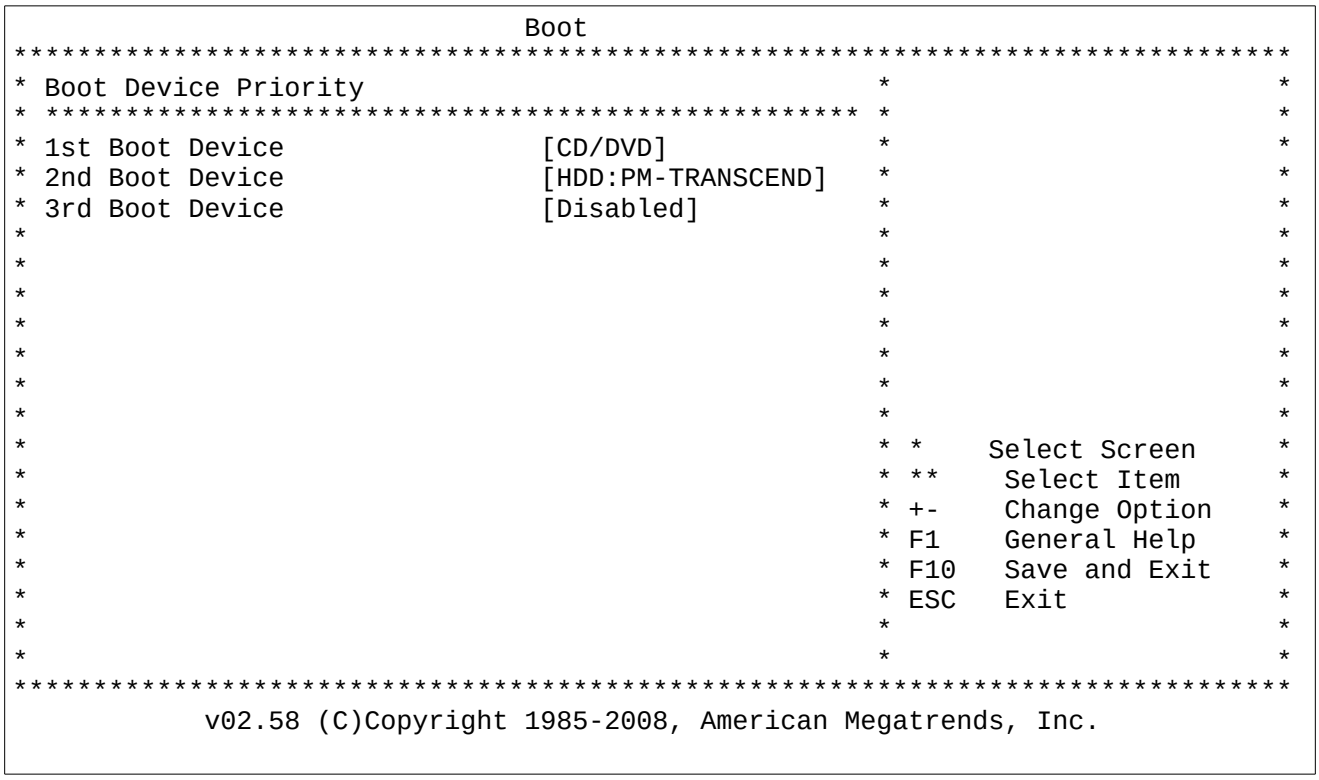


Figure 12: Boot Priority Overall.

This page displays the first device set under each category and allows to change the boot priority order.

12.12 Boot Priority for Hard-drive

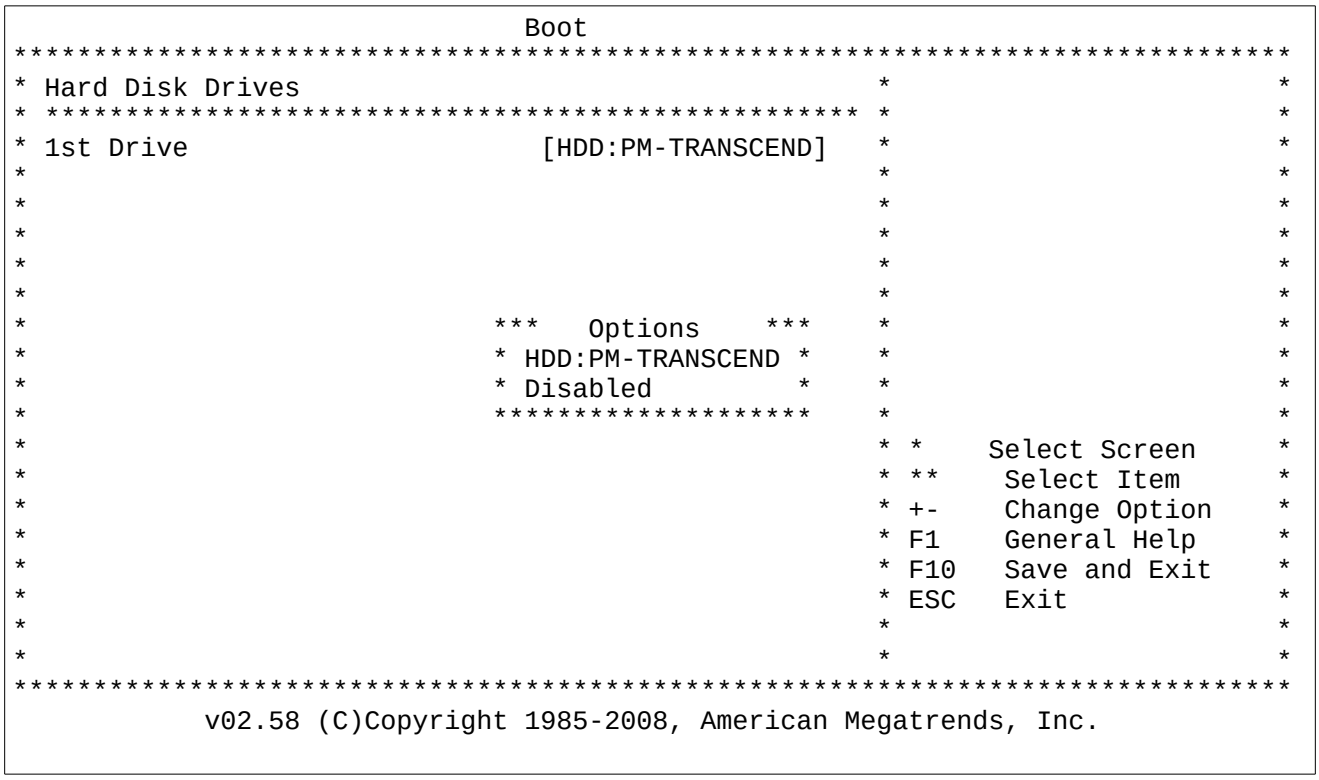


Figure 13: Boot Priority for Hard-drive.

This page displays all the detected IDE devices and allows to change the boot priority order.

12.13 Boot Priority for Removable Device

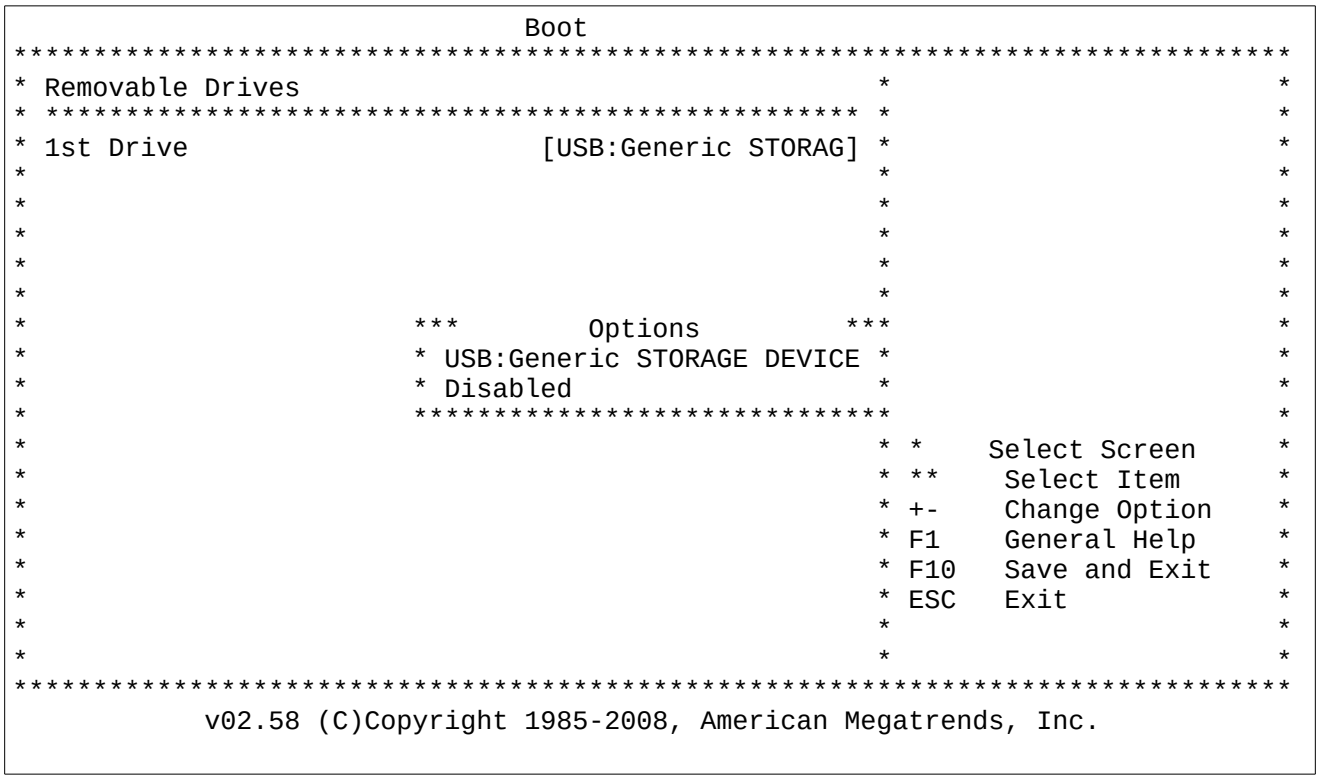


Figure 14: Boot Priority for Removable Device.

This page displays all the detected removable devices and allows to change the boot priority order.

12.14 Security Configuration

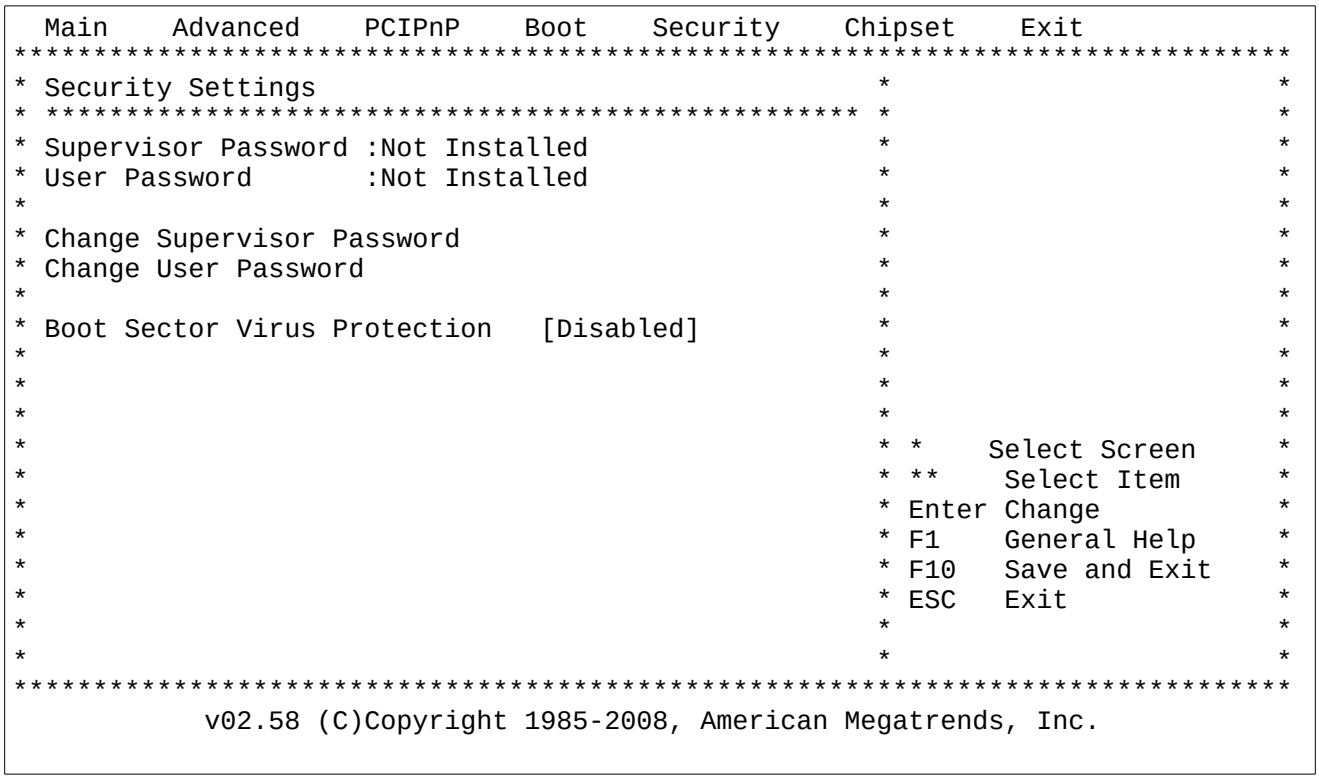


Figure 15: Security Configuration.

The Security Configuration page allows to protect the BIOS setting with a password.

Supervisor Password: show if a supervisor password was created.
User Password: show if a user password was created.

Change Supervisor Password: create/change the supervisor password.
Change User Password: create/change the user password.

The supervisor password grants access to all the BIOS settings where the user password restricts the access to some specific BIOS settings. The restriction to some of the BIOS settings by the user is defined at the BIOS image creation. These restrictions can only be modified on the BIOS image file using the AMIBCP tool.

Boot Sector Virus Protection: prevent/allow write access to the boot sector.

12.15 Chipset sub-menu

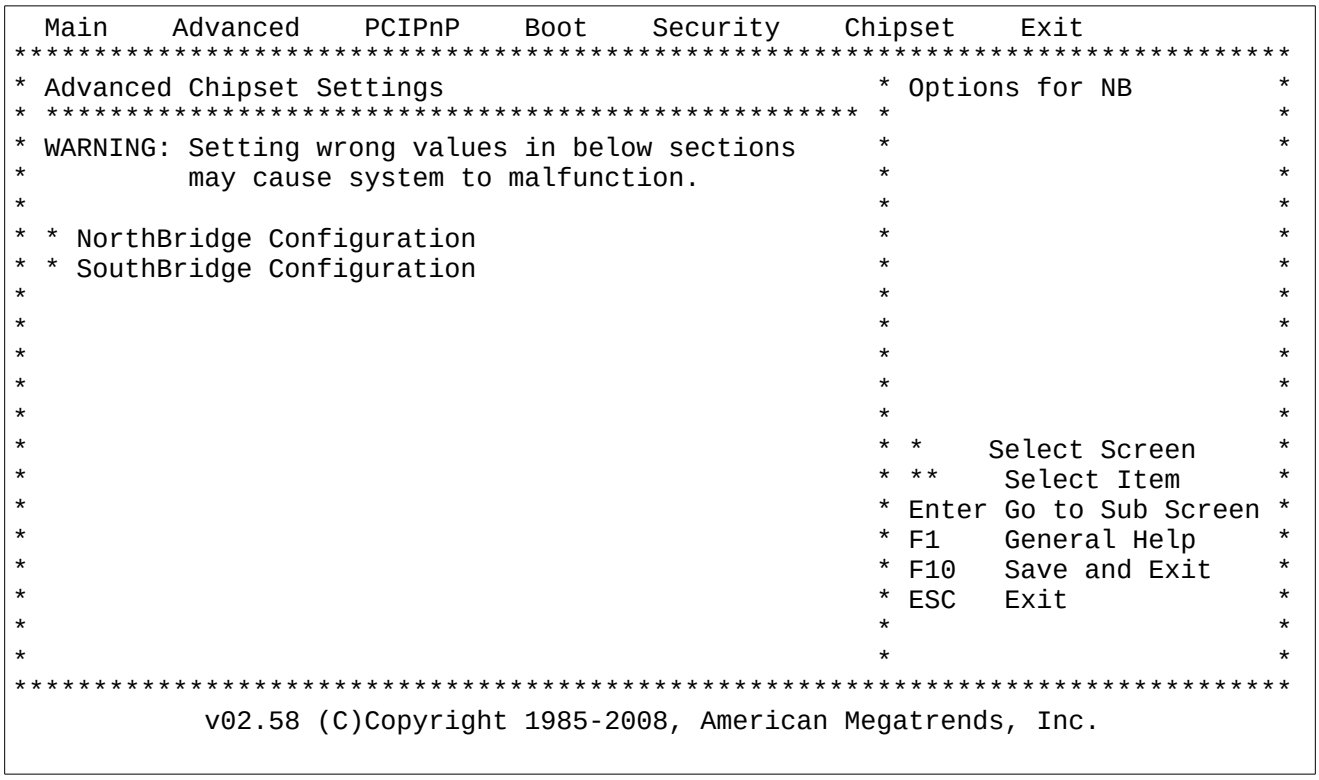


Figure 16: Chipset sub-menu.

The Chipset settings page provides:

- Access to the NorthBridge configuration sub-menu.
- Access to the SouthBridge configuration sub menu.

12.16 NorthBridge Configuration

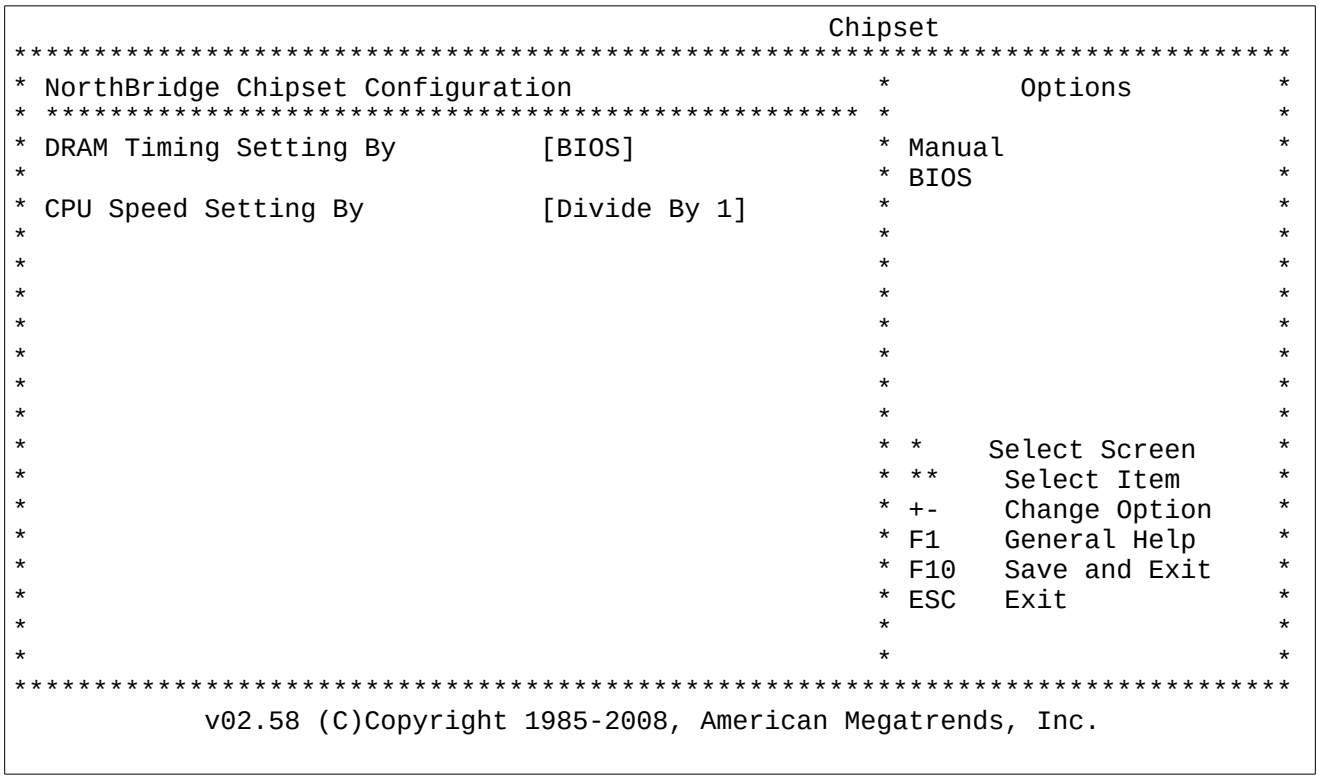


Figure 17: NorthBridge Configuration.

The NorthBridge configuration page provides:

- Access to the DRAM timing settings.
- Access to the CPU clock speed settings.

DRAM Timing Setting By: select if the memory timing is set by the BIOS or manually.

Any mis-configuration of the DRAM timing can prevent the system from working properly.

CPU Speed Setting By: select the CPU clock speed by dividing the base CPU clock of 300MHz with a factor from 1 to 8.

12.17 SouthBridge Configuration

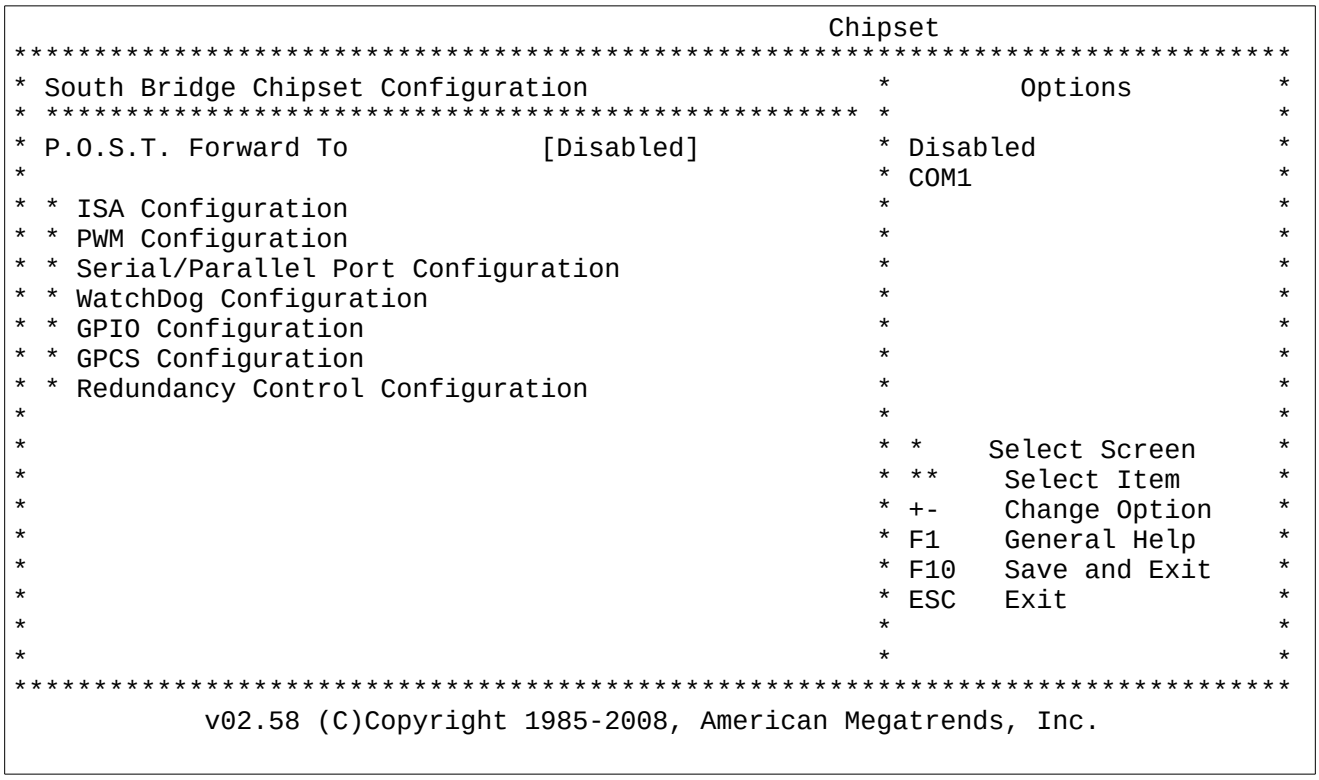


Figure 18: SouthBridge Configuration.

The SouthBridge configuration page provides:

- P.O.S.T. Code to be redirected to COM1.
- Access to the ISA clock timing configuration.
- Access to the Serial and Parallel ports configuration.
- Access to the WatchDog configuration.
- Access to the General Purpose Input/Output configuration.
- Access to the General Purpose Chip Select configuration.
- Access to the Redundancy control configuration.

12.18 ISA Clock settings

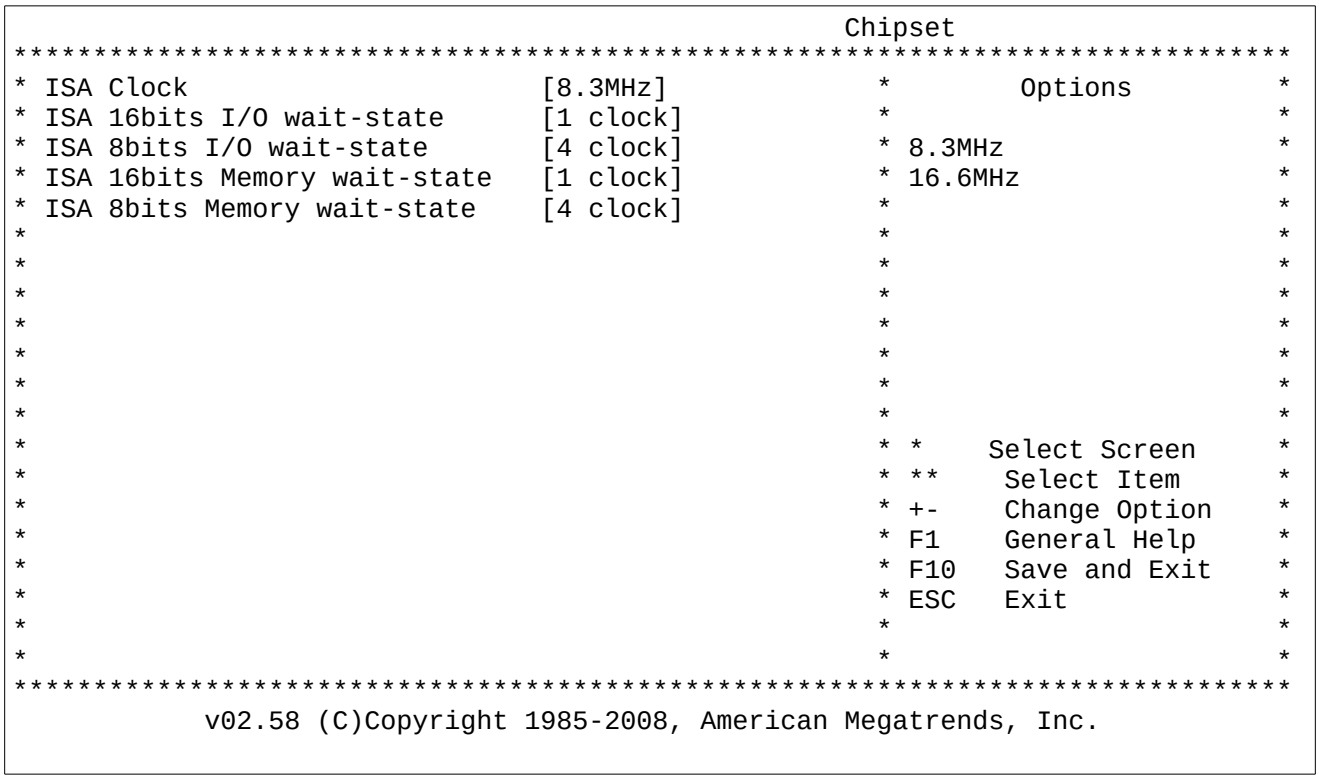


Figure 19: ISA Clock Settings.

The ISA Clock settings page allows to configure the ISA clock and the wait-state of the different ISA operations.

ISA Clock: allow to configure the ISA clock to 8.3MHz or 16.6MHz.
ISA 16bits I/O wait-state: set the duration for the wait-state of a 16bits I/O operation.
ISA 8bits I/O wait-state: set the duration for the wait-state of a 8bits I/O operation.
ISA 16bits Memory wait-state: set the duration for the wait-state of a 16bits memory operation.
ISA 8bits Memory wait-state: set the duration for the wait-state of a 8bits memory operation.

12.19 PWM Timers Configuration

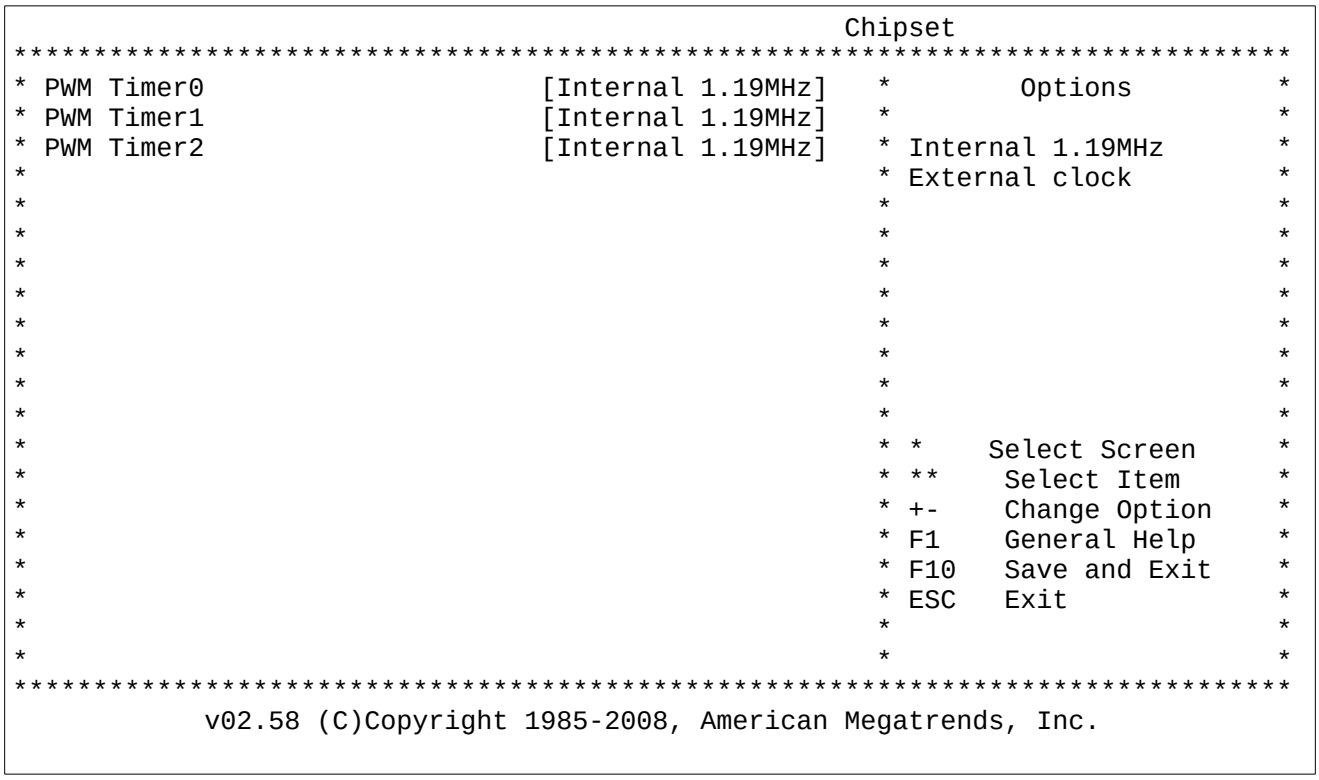


Figure 20: PWM Timers Configuration.

The PWM Timers Configuration page allows to select the source clock for each PWM.

PWM Timer0: select the PWM 0 Timer clock source between the internal 1.19MHz or from the external clock input.
PWM Timer1: select the PWM 1 Timer clock source between the internal 1.19MHz or from the external clock input.
PWM Timer2: select the PWM 2 Timer clock source between the internal 1.19MHz or from the external clock input.

12.20 Serial/Parallel Ports Configuration

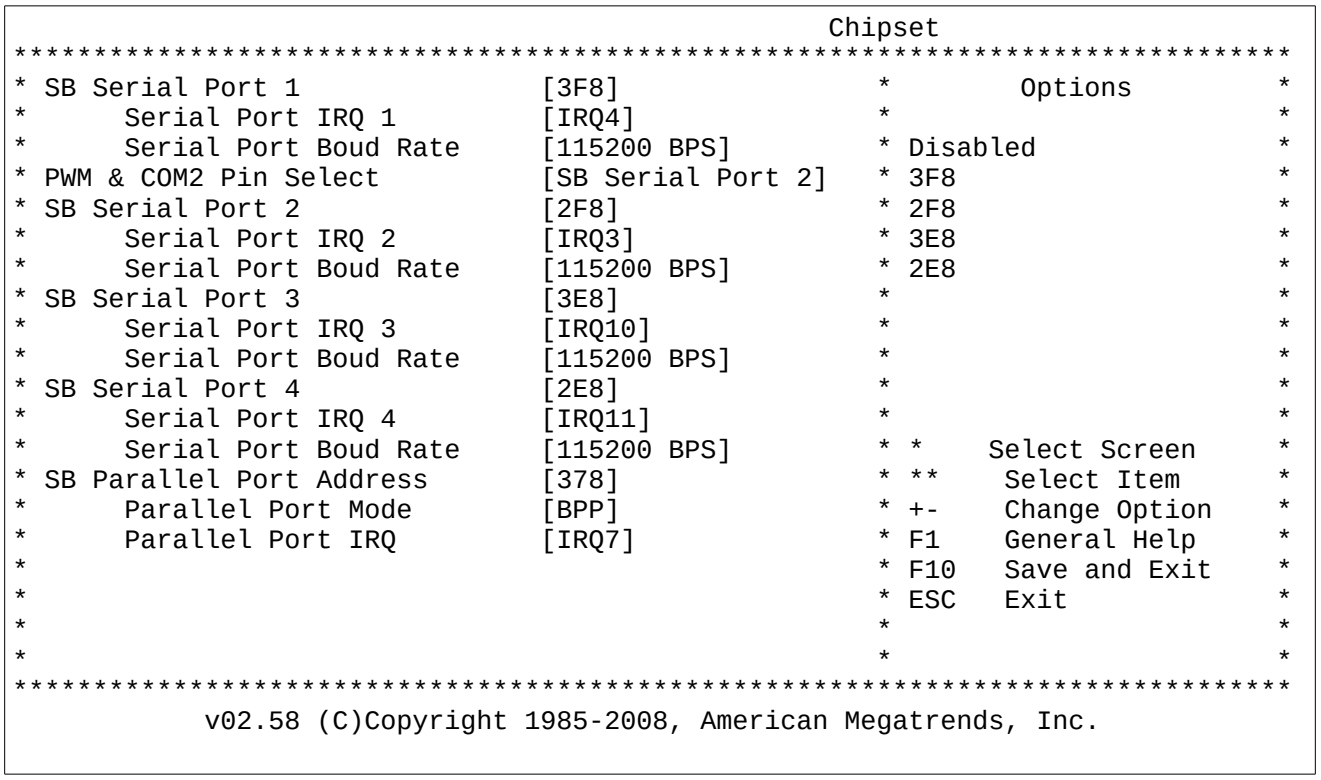


Figure 21: Serial/Parallel Ports Configuration.

The Serial/Parallel Ports Configuration page provides the base configuration for the four serial ports and the parallel port.

SB Serial Port 1: select the base address for the physical serial port 1.
Serial Port IRQ 1: select the interrupt for the physical serial port 1.
Serial Port Baud Rate: select the initial baud rate for the physical serial port 1.

PWM & COM2 Pin Select: select if the pins of COM2 are used as serial port or as PWM.
SB Serial Port 2: select the base address for the physical serial port 2.
Serial Port IRQ 2: select the interrupt for the physical serial port 2.
Serial Port Baud Rate: select the initial baud rate for the physical serial port 2.

SB Serial Port 3: select the base address for the physical serial port 3.
Serial Port IRQ 3: select the interrupt for the physical serial port 3.
Serial Port Baud Rate: select the initial baud rate for the physical serial port 3.

SB Serial Port 4: select the base address for the physical serial port 4.

Serial Port IRQ 4: select the interrupt for the physical serial port 4.
Serial Port Baud Rate: select the initial baud rate for the physical serial port 4.

SB Parallel Port Address: select the base address for the parallel port.
Serial Port Mode: select the parallel port mode between, SPP, BPP, EPP and ECP.
Serial Port IRQ: select the interrupt for the parallel port.
EPP Version: select between EPP compatibility mode 1.7 and 1.9.
ECP Mode DMA Channel: select the DMA channel assigned to the parallel port.

12.21 Watchdogs Configuration

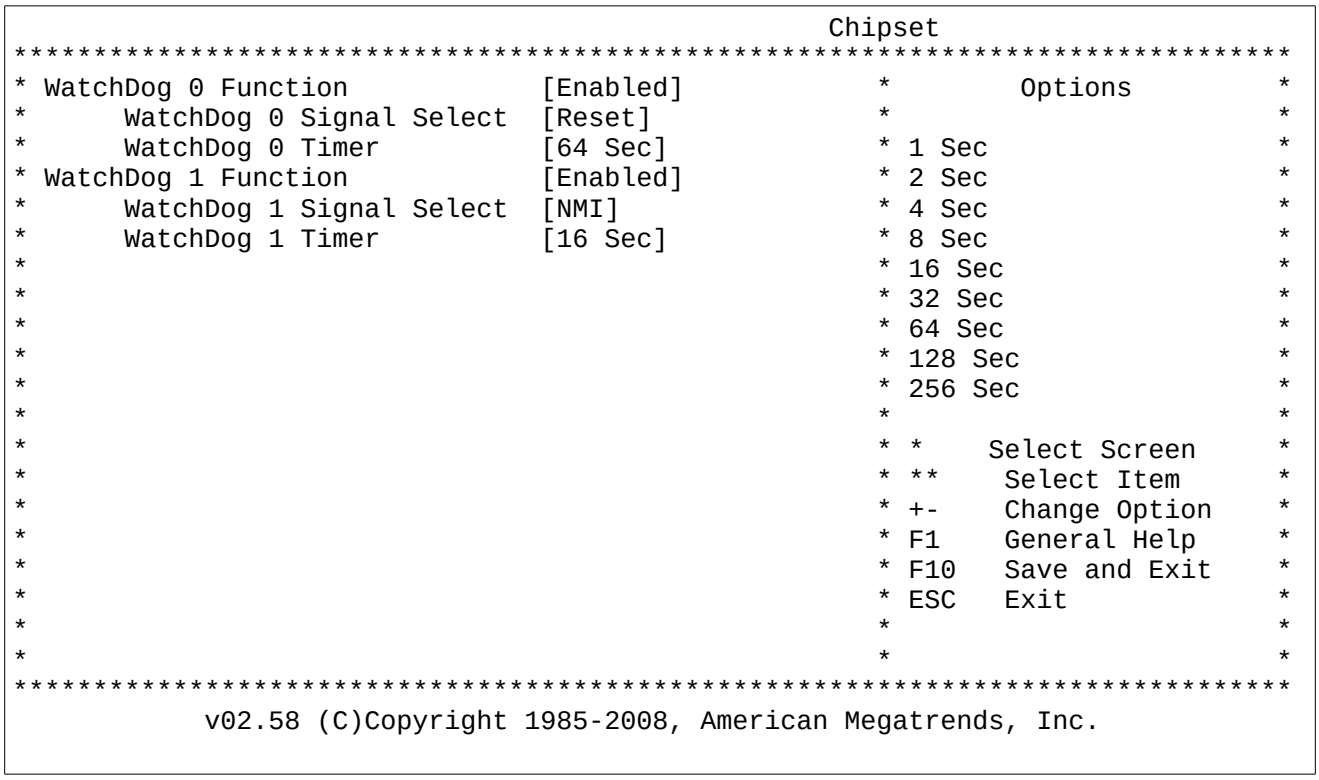


Figure 22: Watchdogs Configuration.

The WatchDog Configuration page allows to select the event and the delay for each WatchDog when activated.

WatchDog 0 Function: enable/disable the watchdog timer 0.
WatchDog 0 Signal Select: select the event generated when the watchdog 0 occurs.
WatchDog 0 Timer: set the delay in seconds before the watchdog 0 occurs.

WatchDog 1 Function: enable/disable the watchdog timer 1.
WatchDog 1 Signal Select: select the event generated when the watchdog 1 occurs.
WatchDog 1 Timer: set the delay in seconds before the watchdog 1 occurs.

12.22 GPIO Ports sub-menu

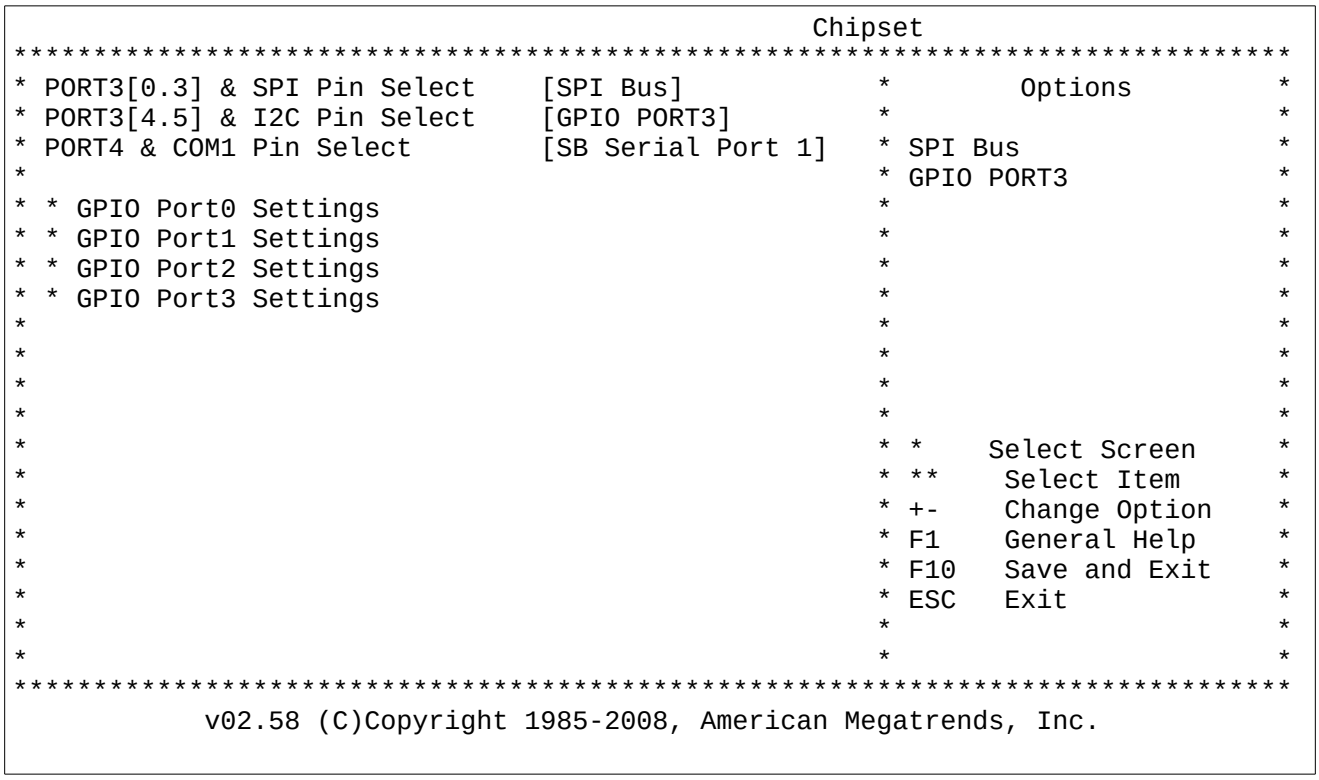


Figure 23: GPIO Ports sub-menu.

The GPIO ports sub-menu allows to:

- Select the share functionality of the GPIO port 3.
- Select the share functionality of the GPIO port 4.
- Access to sub-menu for each individual GPIO port settings.

PORT3 [0.3] & SPI Pin Select: select if the pin 15 to 18 of connector CN16 are assigned to SPI or GPIO port 3.
PORT3 [4.5] & SPI Pin Select: feature not available on the Vortex86SX.
PORT4 & COM1 Pin Select: select if the pins of the 1st connector CN8 are assigned to COM1 or GPIO port 4

There is some limitation to use PORT4 as GPIO because it is wired to the connector CN8 through an RS232 transceiver.

12.23 GPIO Port 0 Configuration

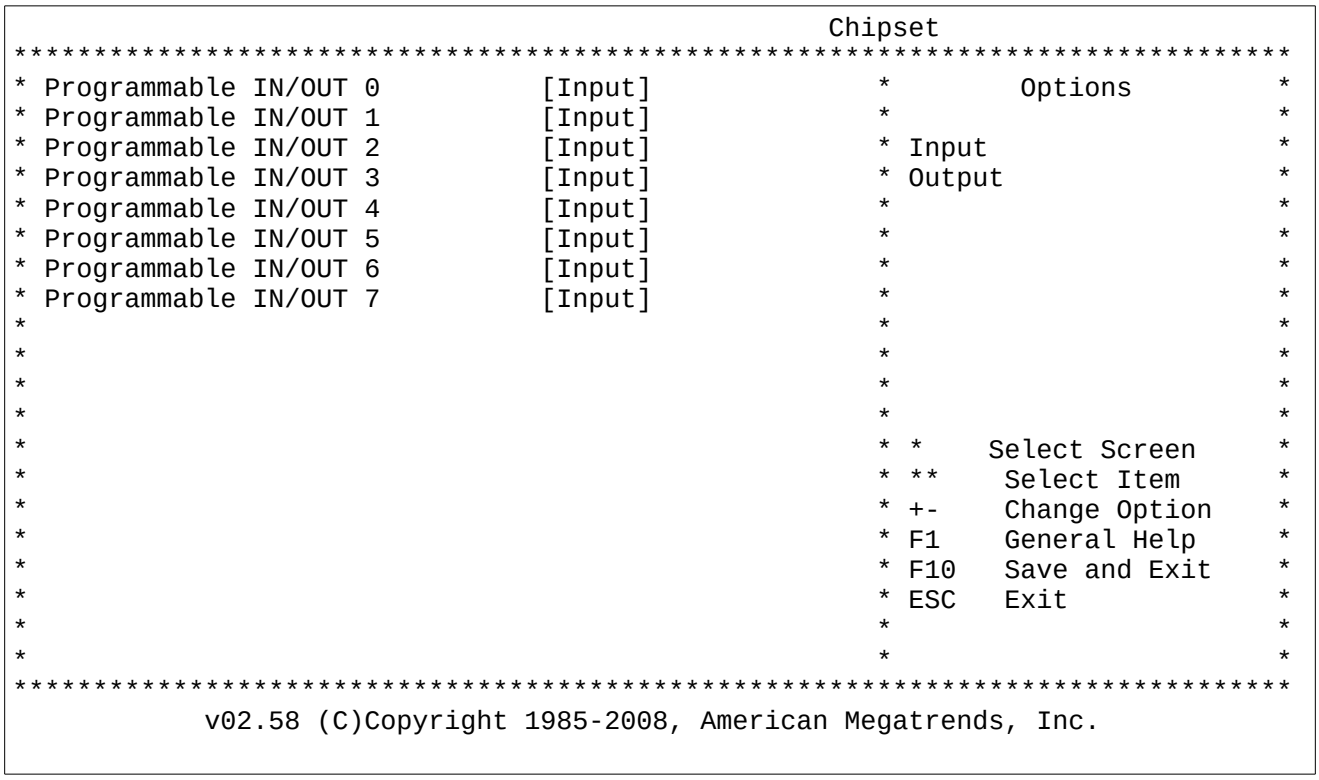


Figure 24: GPIO Port 0 Configuration.

The GPIO Port 0 Configuration page allows to set each pin of the port 0 as input or output and define the default value when acting as output.

Programmable IN/OUT 0: select if the pin 1 of connector CN26 is set as input or output.
Output Value: select if the pin is set to 0 or 1 when assigned as output.

Programmable IN/OUT 1: select if the pin 2 of connector CN26 is set as input or output.
Output Value: select if the pin is set to 0 or 1 when assigned as output.

Programmable IN/OUT 2: select if the pin 3 of connector CN26 is set as input or output.
Output Value: select if the pin is set to 0 or 1 when assigned as output.

Programmable IN/OUT 3: select if the pin 4 of connector CN26 is set as input or output.
Output Value: select if the pin is set to 0 or 1 when assigned as output.

Programmable IN/OUT 4: select if the pin 5 of connector CN26 is set as input or output.
Output Value: select if the pin is set to 0 or 1 when assigned as output.

Programmable IN/OUT 5: select if the pin 6 of connector CN26 is set as input or output.
Output Value: select if the pin is set to 0 or 1 when assigned as output.

Programmable IN/OUT 6: select if the pin 7 of connector CN26 is set as input or output.
Output Value: select if the pin is set to 0 or 1 when assigned as output.

Programmable IN/OUT 7: select if the pin 8 of connector CN26 is set as input or output.
Output Value: select if the pin is set to 0 or 1 when assigned as output.

12.24 GPIO Port 1 Configuration

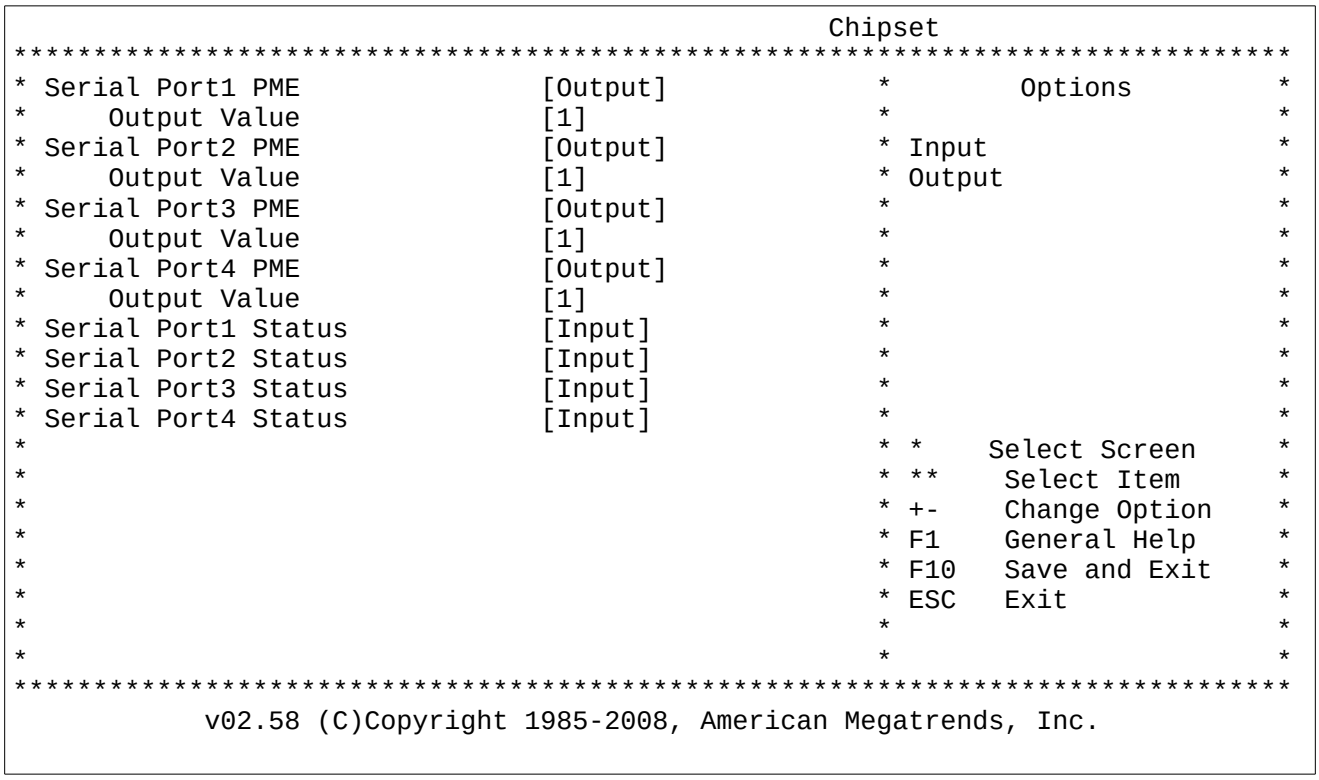


Figure 25: GPIO Port 1 Configuration.

The GPIO Port 1 Configuration page provides power management control for the RS232 transceiver of the four physical serial ports.

Serial Port1 PME: set as output to control the transceiver of the serial port 1.
set as input force the factory default.
Output Value: 0 set the transceiver in power save until valid RS232 level is detected.
1 force the transceiver ON.

Serial Port2 PME: set as output to control the transceiver of the serial port 2.
set as input force the factory default.
Output Value: 0 set the transceiver in power save until valid RS232 level is detected.
1 force the transceiver ON.

Serial Port3 PME: set as output to control the transceiver of the serial port 3.
set as input force the factory default.
Output Value: 0 set the transceiver in power save until valid RS232 level is detected.
1 force the transceiver ON.

Serial Port4 PME: set as output to control the transceiver of the serial port 4.
set as input force the factory default.
Output Value: 0 set the transceiver in power save until valid RS232 level is detected.
1 force the transceiver ON .

Serial Port 1 Status: this setting must be set always as input.
used to read the RS232 transceiver status of the serial port 1.
read 0 when no valid RS232 level applied to any of CN8 inputs.
read 1 when a valid RS232 level is applied to at least one input of CN8.

Serial Port 2 Status: this setting must be set always as input.
used to read the RS232 transceiver status of the serial port 2.
read 0 when no valid RS232 level applied to any of CN9 inputs.
read 1 when a valid RS232 level is applied to at least one input of CN9.

Serial Port 3 Status: this setting must be set always as input.
used to read the RS232 transceiver status of the serial port 3.
read 0 when no valid RS232 level applied to any of CN11 inputs.
read 1 when a valid RS232 level is applied to at least one input of CN11.

Serial Port 4 Status: this setting must be set always as input.
used to read the RS232 transceiver status of the serial port 4.
read 0 when no valid RS232 level applied to any of CN10 inputs.
read 1 when a valid RS232 level is applied to at least one input of CN10.

12.25 GPIO Port 2 Configuration

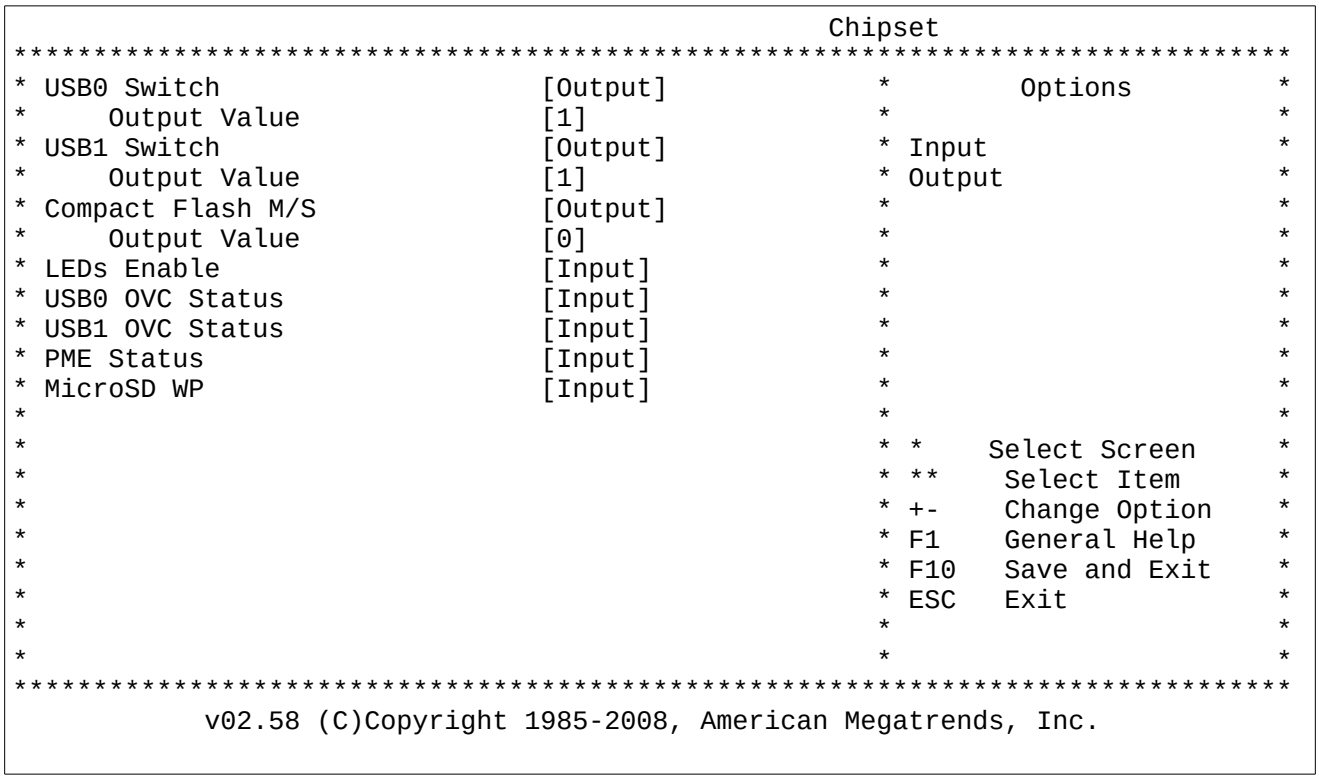


Figure 26: GPIO Port 2 Configuration.

The GPIO Port 2 Configuration page provides control for the power switches of the external USB ports and the selection for the Compact Flash Slot to Master or Slave.

USB0 Switch: set as output to control power switch of the USB port 0.
set as input force the factory default.
Output Value: 0 turn the power switch of the USB port 0 OFF.
1 turn the power switch of the USB port 0 ON.

USB1 Switch: set as output to control power switch of the USB port 1.
set as input force the factory default.
Output Value: 0 turn the power switch of the USB port 1 OFF.
1 turn the power switch of the USB port 1 ON.

Compact Flash M/S: set as output to control the mode of the Compact Flash Slot.
set as input force the factory default.
Output Value: 0 set the compact Flash Slot to Primary Master.
1 set the compact Flash Slot to Primary Slave.

LEDs Enable: enable/disable the on-board LEDs.
set as input force the factory default.
Output Value: 0 enable the on-board LEDs.
1 disable the on-board LEDs

USB 0 OVC Status: this setting must be set always as input.
used to read the power switch status of the USB port 0.
read 0 when the power switch over current flag is set.
read 1 when the power switch is operating normally.

USB 1 OVC Status: this setting must be set always as input.
used to read the power switch status of the USB port 1.
read 0 when the power switch over current flag is set.
read 1 when the power switch is operating normally.

PME Status: this setting must be set always as input.
used to read if a power management event occurred on the PCI bus.
read 0 when a power management event has occurred on the PCI bus.
read 1 when no power management event has occurred on the PCI bus.

MicroSD WP: allow to write protect the on-board Micro-SD.
set as input force the factory default.
Output Value: 0 allow to write to the Micro-SD.
1 the Micro-SD is write protected.

12.26 GPIO Port 3 Configuration

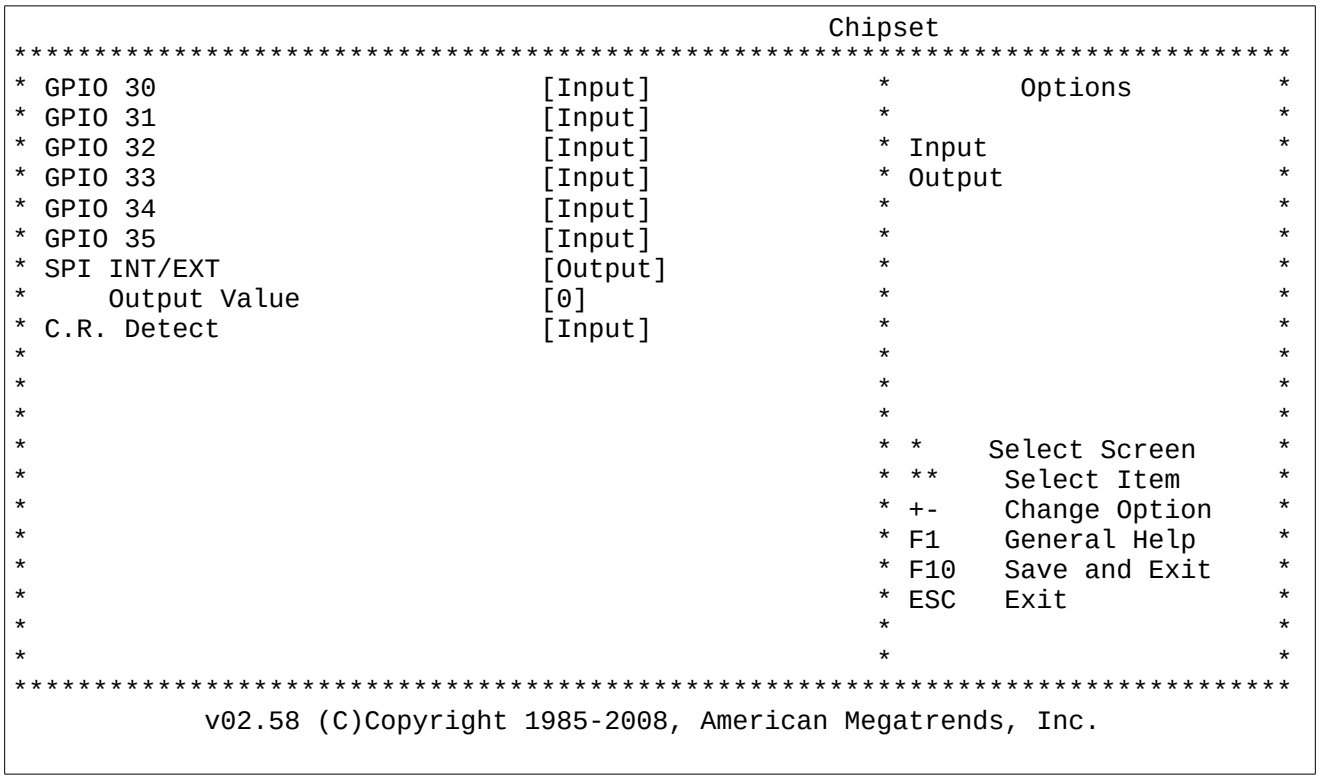


Figure 27: GPIO Port 3 Configuration.

The GPIO Port 3 Configuration page allows to set each pin of the port 3 as input or output and define the default value when acting as output. Some settings can be unavailable when the pin is assigned to an alternate functionality.

GPIO 30: select if the pin 4 of connector CN17 is set as input or output.
Output Value: select if the pin is set to 0 or 1 when assigned as output.
feature unavailable when the pin is assigned to the SPI port.

GPIO 31: select if the pin 3 of connector CN17 is set as input or output.
Output Value: select if the pin is set to 0 or 1 when assigned as output.
feature unavailable when the pin is assigned to the SPI port.

GPIO 32: select if the pin 1 of connector CN17 is set as input or output.
Output Value: select if the pin is set to 0 or 1 when assigned as output.
feature unavailable when the pin is assigned to the SPI port.

GPIO 33: select if the pin 2 of connector CN17 is set as input or output.
Output Value: select if the pin is set to 0 or 1 when assigned as output.
feature unavailable when the pin is assigned to the SPI port.

GPIO 34: select if the pin 2 of connector CN16 is set as input or output.
Output Value: select if the pin is set to 0 or 1 when assigned as output.

GPIO 35: select if the pin 3 of connector CN16 is set as input or output.
Output Value: select if the pin is set to 0 or 1 when assigned as output.

SPI INT/EXT: select if the SPI port access the on-board SPI flash or SPI connector CN17.
set as input force the factory default.
Output Value: 0 access the on-board SPI flash.
1 access the SPI connector CN17.

C.R. Detect: used by the BIOS to force the Console Redirection On, even when disable in the BIOS setting.

12.27 GPIO Port 4 Configuration

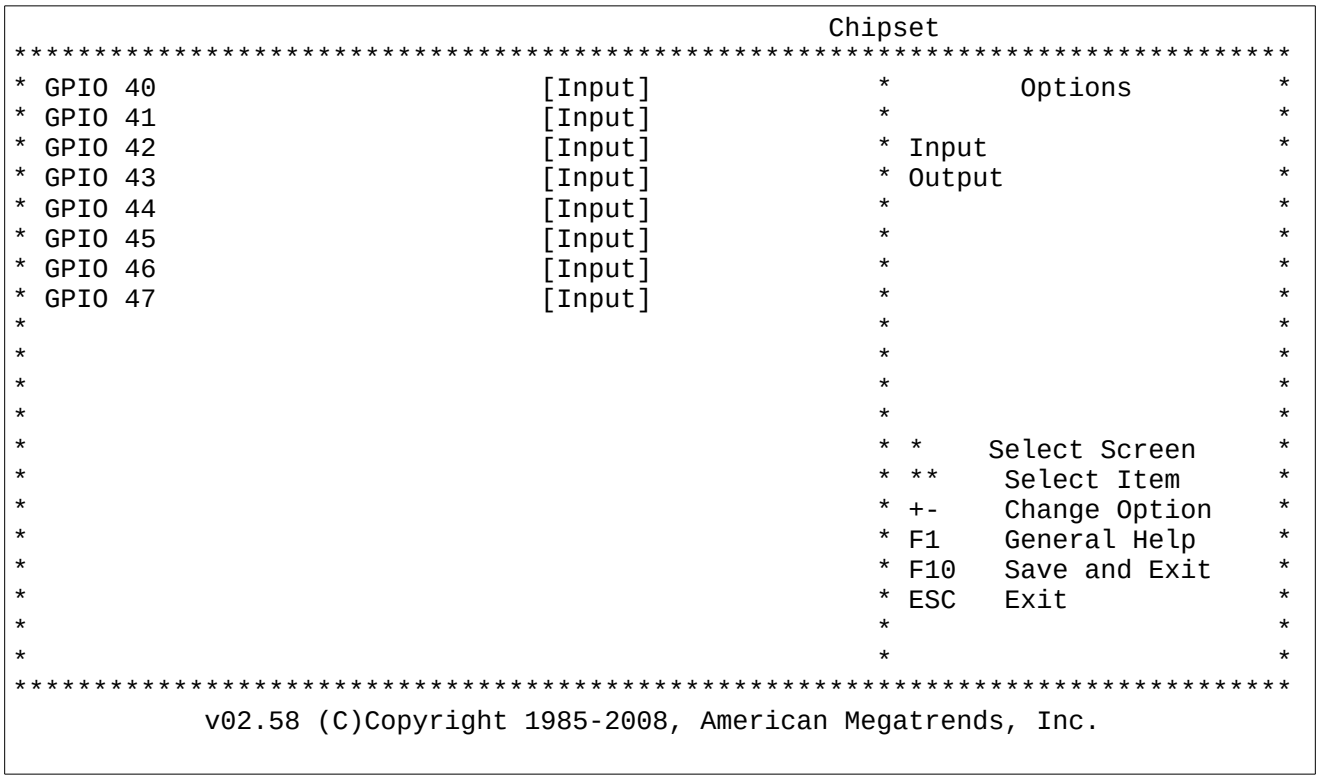


Figure 28: GPIO Port 4 Configuration.

The GPIO Port 4 Configuration page allows to set each pin of the port 4 as input or output and define the default value when acting as output. The settings for this port are unavailable when the pins are used for the serial port COM1.

GPIO 40: This setting must be set always as input.
Use to read the RS232 level on connector CN8 pin 1.
read 0 when RS232 level is high.
read 1 when RS232 level is low.
Feature unavailable when the pin is assigned to COM1.

GPIO 41: This setting must be set always as output.
Output Value: drive the connector CN8 pin 5 to an RS232 level high or low.
0 drive the RS232 level high.
1 drive the RS232 level low.
Feature unavailable when the pin is assigned to COM1.

GPIO 42: This setting must be set always as output.
Output Value: drive the connector CN8 pin 4 to an RS232 level high or low.
0 drive the RS232 level high.
1 drive the RS232 level low.
Feature unavailable when the pin is assigned to COM1.

GPIO 43: This setting must be set always as input.
Use to read the RS232 level on connector CN8 pin 8.
read 0 when RS232 level is high.
read 1 when RS232 level is low.
Feature unavailable when the pin is assigned to COM1.

GPIO 44: This setting must be set always as input.
Use to read the RS232 level on connector CN8 pin 3.
read 0 when RS232 level is high.
read 1 when RS232 level is low.
Feature unavailable when the pin is assigned to COM1.

GPIO 45: This setting must be set always as output.
Output Value: drive the connector CN8 pin 7 to an RS232 level high or low.
0 drive the RS232 level high.
1 drive the RS232 level low.
Feature unavailable when the pin is assigned to COM1.

GPIO 46: This setting must be set always as input.
Use to read the RS232 level on connector CN8 pin 2.
read 0 when RS232 level is high.
read 1 when RS232 level is low.
Feature unavailable when the pin is assigned to COM1.

GPIO 47: This setting must be set always as input.
Use to read the RS232 level on connector CN8 pin 6.
read 0 when RS232 level is high.
read 1 when RS232 level is low.
Feature unavailable when the pin is assigned to COM1.

12.28 GPCS Configuration

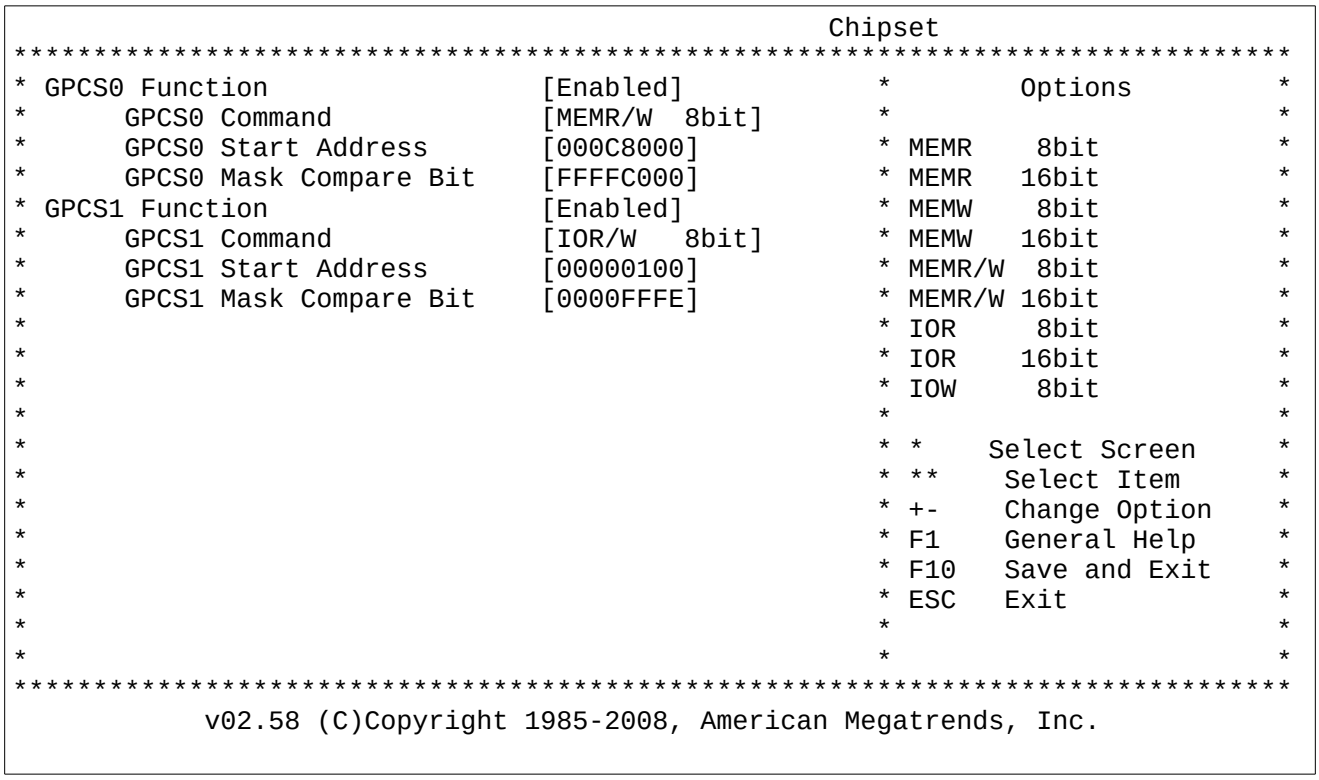


Figure 29: GPCS Configuration.

The GPCS Configuration page provides the settings for the two external General Purpose Chip Select.

GPCS0 Function: enable/disable the function on the connector CN16 pin 8.
- **GPCS0 Command:** select during which operation the chip select is activated.
- **GPCS0 Start Address:** define the base address of the chip select.
- **GPCS0 Mask Compare Bit:** define the address window where the chip select is active.

GPCS1 Function: enable/disable the function on the connector CN16 pin 9.
- **GPCS1 Command:** select during which operation the chip select is activated.
- **GPCS1 Start Address:** define the base address of the chip select.
- **GPCS1 Mask Compare Bit:** define the window size where the chip select is active.

12.29 Redundancy Port Configuration

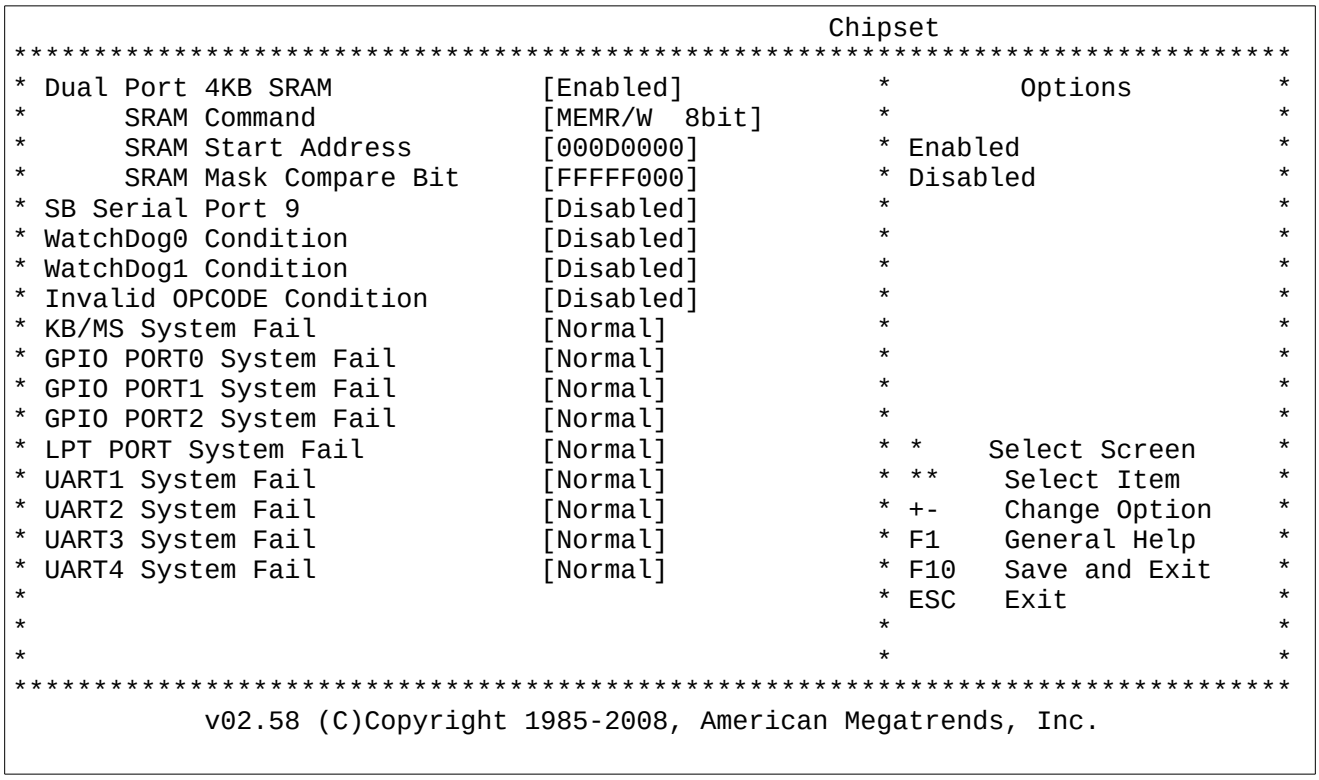


Figure 30: Redundancy Port Configuration.

This page allows to configure the communication ports and the fail conditions of the redundancy port. It also allow to define fail state for some devices.

Dual Port 4KB SRAM: enable /disable the internal dual port 4KB SRAM.
- **SRAM Command:** define the access mode of the SRAM.
- **SRAM Start Address:** define the base address of the SRAM.
- **SRAM Mask Compare Bit:** set the windows size of the SRAM used

SB Serial Port 9: set the base address of the serial port 9.
- **Serial Port IRQ 9:** set the interrupt assigned to serial port 9.

WatchDog0 Condition: enable/disable watchdog 0 as fail condition.

WatchDog1 Condition: enable/disable watchdog 1 as fail condition.

Invalid OPCODE Condition: enable/disable an invalid OPCODE as fail condition.

KB/MS System Fail: allows to set both PS/2 ports to tri-state when a failure occurs.

GPIO Port0 System Fail: allows to set the GPIO port 0 to tri-state when a failure occurs.

GPIO Port1 System Fail: allows to set the GPIO port 1 to tri-state when a failure occurs.

GPIO Port2 System Fail: allows to set the GPIO port 2 to tri-state when a failure occurs.

GPIO Port0 System Fail: allows to set the GPIO port 0 to tri-state when a failure occurs.

LPT PORT System Fail: allows to set the parallel port to tri-state when a failure occurs.

UART1 System Fail: allows to set the serial port 1 to tri-state when a failure occurs.

UART2 System Fail: allows to set the serial port 2 to tri-state when a failure occurs.

UART3 System Fail: allows to set the serial port 3 to tri-state when a failure occurs.

UART4 System Fail: allows to set the serial port 4 to tri-state when a failure occurs.

Only the port of the CPU will be tri-stated, these settings do not control the RS232 transceivers. The RS232 transceiver are disabled automatically with the signal SYS-FAIL-OUT.

12.30 Exit Options

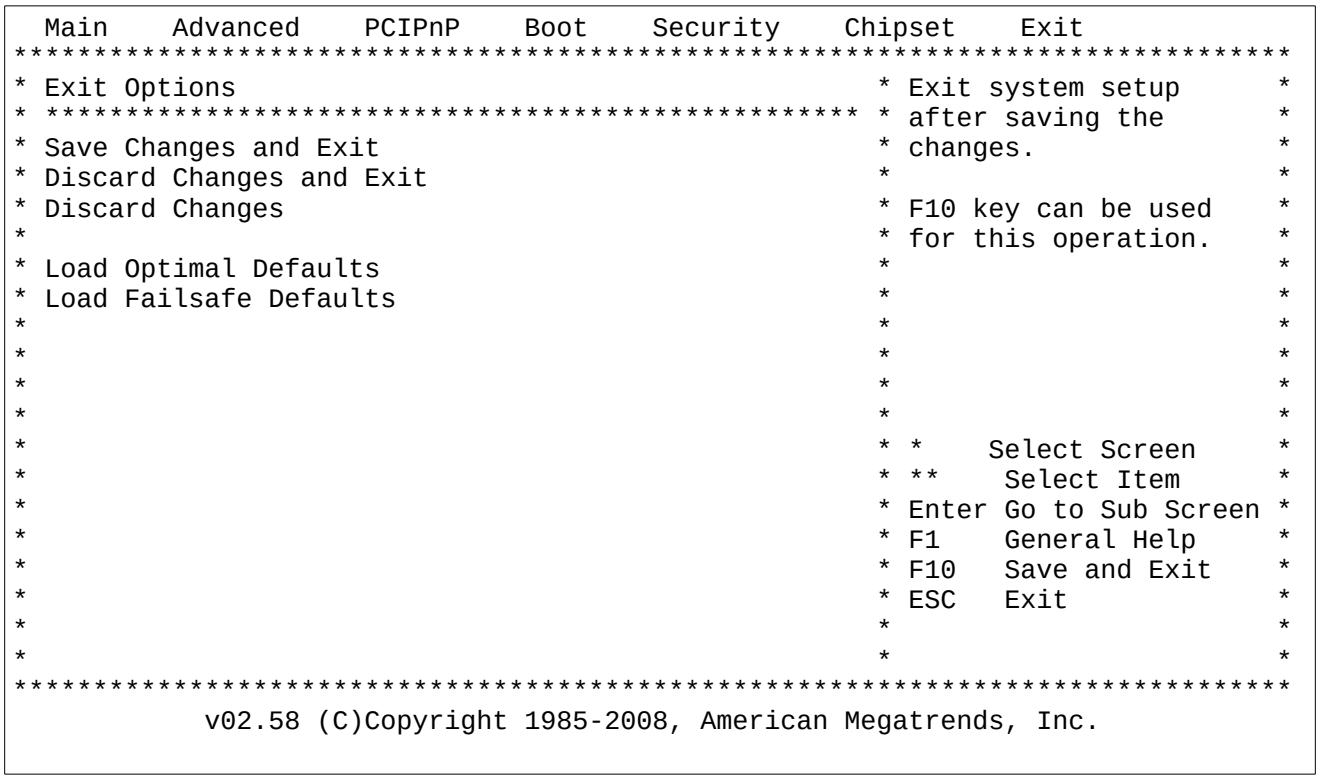


Figure 31: Exit Options.

The Exit Options page allows to reload the default BIOS settings and exit the BIOS setting saving or discarding the changes.

Save Changes and exit: save all changes and exit the BIOS setting.
Discard Changes and exit: discard all changes and exit the BIOS setting.
Discard Changes: reset all changes back to previously saved value.

Load Optimal Defaults: load in the NVRAM the Optimal settings pre-programmed into the BIOS.
Load Failsafe Defaults: load in the NVRAM the Failsafe settings pre-programmed into the BIOS.

The BIOS flash contains two default configurations, one as optimal and one as failsafe. Both configurations are defined at the BIOS image creation and can only be modified on the BIOS image file using the AMIBCP tool.

CHAPTER 13: Literature REFERENCES

The following references are for information about the PC/104 architecture, the PC DOS, and the PC BIOS.

13.1 ISA System Architecture

MindShare, Inc., Tom Shanley and Don Anderson
Internet: mindshar@interserv.com
CompuServe: 72507,1054
Published by Addison Wesley, Inc.

13.2 AT Bus Design

Edward Solari
Anabooks
12145 Alta Carmel Ct., Suite 250
San Diego, CA 92128
ISBN 0-929392-08-6

13.3 Personal Computer Bus Standard P996

Institute of Electrical and Electronic Engineers, Inc.
445 Hoes Lane
Piscataway, NJ 08854

13.4 PC Interrupts

PC Interrupts, Ralf Brown, Addison/Wesley.

13.5 PC/104 Consortium

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