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TMZ104-V2.5

User Manual

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Warning

- A working knowledge of electronics and PC-technology is required to use this product.
- Pay attention to electrostatic discharges. Use a CMOS protected workplace.
- Disconnect power source when connecting any cables or devices.

This is a high-technology product.
A working knowledge of electronics and PC-technology is required!

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CHAPTER 1: GENERAL DESCRIPTION

The TMZ104 is a PC/104 compliant system controller measuring just 3.55 inches by 3.775 inches. The TMZ104 offers the quickest route of integrating a full x86 AT-compatible computer into your embedded control application using the PC/104 form factor. In addition, the built-in peripherals minimize the number of additional modules required. By combining the system hardware, I/O, software (integrated RTOS image) and solid-state mass storage, the TMZ104 lowers your exposure to possible development risks, costs and significantly reduces your time-to-market.

The TMZ104's full compatibility with the popular PC/104 embedded expansion bus allows you to easily integrate the widest selection of low-cost hardware peripherals. The numerous features provide an ideal price/performance solution.

1.1 Specifications

1.1.1 Transmeta Crusoe 5500

- 128 bit instruction set VLIW processor and x86 Code Morphing™ software running from 333 to 533 MHz
- Integrated 64KB L1 instruction cache, 64KB L1 data cache, and 256KB L2 write-back cache
- Integrated floating point unit
- Integrated Northbridge
- MMX2 compatible

1.1.2 PC Core Logic with PCI enhancement

- 32 bit 33MHz PCI rev 2.1 compliant "Northbridge" and "Southbridge"
- AT-compatible DMA controllers, interrupt controllers, timer/counters
- AT keyboard controller and Real-time clock

1.1.3 Memory

- Synchronous DRAM support
- Onboard 144-pin SO-DIMM socket for up to 256MB SDRAM

1.1.4 Universal Serial Bus

- One independent USB interface, USB 1.1 UHCI compliant
- PCI bus master burst reads and writes
- Over current and power control support

1.1.5 Serial Ports

- Two 16550-compatible RS232 serial ports
- Baud rates up to 115.2 K baud

1.1.6 Parallel Ports

- One enhanced bi-directional parallel port
- Supports SPP, ECP and EPP

1.1.7 Keyboard/Mouse Interface

- Supports AT keyboard and PS/2 mouse

1.1.8 FDD Interface

- Supports two floppy disk drives

1.1.9 Enhanced IDE Interface

- One enhanced IDE channel, supports up to two drives (master/slave)
- PCI bus master burst reads and writes
- Ultra DMA and PIO modes (1-4) support

1.1.10 Power Management

- I/O traps and idle timers for peripheral power management
- Hardware and software CPU suspend mode support

1.1.11 Solid State Flash Storage

- One 32-pin DIP socket supports M-System DiskOnChip 2000 and DiskOnChip Millennium

1.1.12 Expansion BUS - ISA PC/104 signals

- Fully compliant 16-bit PC/104 Expansion BUS

1.1.13 Electrical Specifications

- Support for low-power modes via CMS LongRun features

		MEMORY SIZE			
		32MB	64MB	96MB	160MB
SPEED	333MHz @ 1.00V	1.80W	1.84W	2.46W	2.02W
	400MHz @ 1.00V	1.88W	1.93W	2.39W	2.00W
	466MHz @ 1.15V	1.98W	2.03W	2.69W	2.18W
	533MHz @ 1.15V	2.04W	2.04W	2.62W	2.18W

Table 1: TMZ104 Power Consumption (Watts)

The power consumption measurements were performed on a TMZ104 CPU board populated with a DiskOnChip Millennium 8MB running a temperature monitoring program and a shell on a Linux kernel 2.4.

Note: Power consumption figure is averaged with APM disabled.

1.1.14 Mechanical/Environmental

- PC/104 form factor compliant, 3.55" x 3.775 x 0.9" (90mm x 96mm x 23mm)
- Standard PC/104 16-bit stackthrough connector for PC/104-compliant modules
- Standard ribbon cable connectors for IDE, serial, parallel and utilities.
- Operating temperature -40° to 185°F (-40° to 85°C)
- Storage temperature: -67° to 185°F (-55° to 85°C)
- Weight: 0.15 lb. (70G)

CHAPTER 2: EMBEDDED FEATURES

2.1 Dual Watchdog Timer

- Dual mode WDT connected to H/W reset line
- Start up mode with a timeout period of 46.4s (typical)
- Normal mode with a timeout period of 2.9s (typical)
- The WDT can be cleared internally through a GPIO line or externally through the utility connector

2.2 Software included

- AMI embedded PC BIOS – 100% X86 Compatible

2.3 Transmeta LongRun

- The CPU frequency change on the fly depending on the workload
- Reduce the power consumption dramatically on small workload
- Allowed frequencies from 333MHZ to 533MHz.

2.4 On board Battery

- On board battery for RTC clock and CMOS setup.

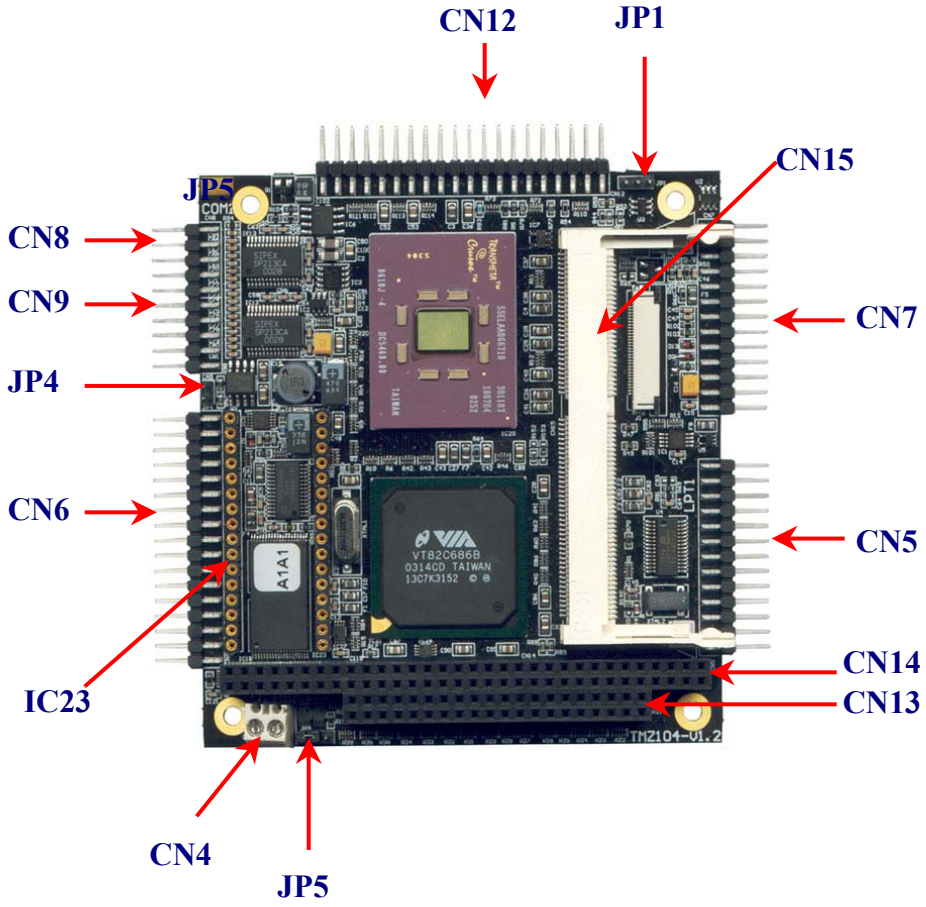
The CPU board needs the battery installed to work properly

2.5 Software Compatibility

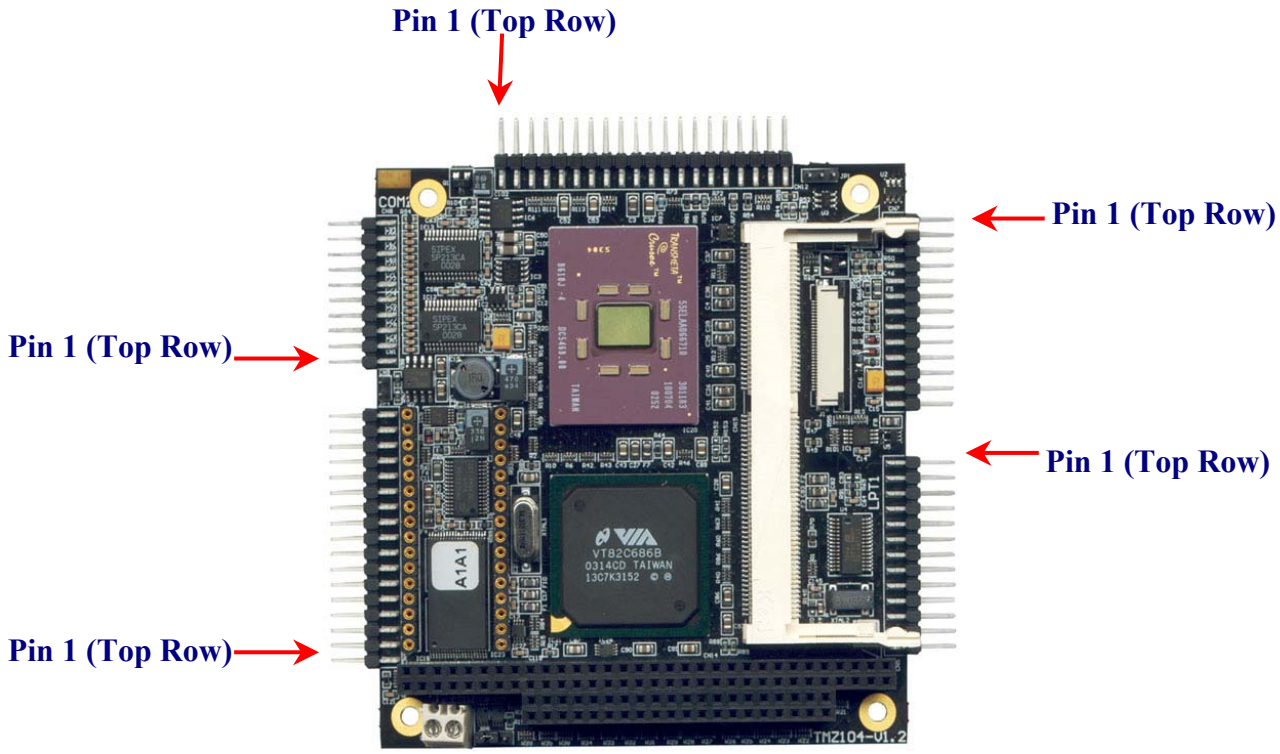
- Linux
- MSDOS 3.X, 4.X, 5.X, 6.X, DRDOS
- Win95/98/NT/2000/XP
- most PC-Compatible RTOS
- WindRiver VxWorks RTOS

CHAPTER 3: INSTALLATION

3.1 Locating the Connectors & JUMPERS



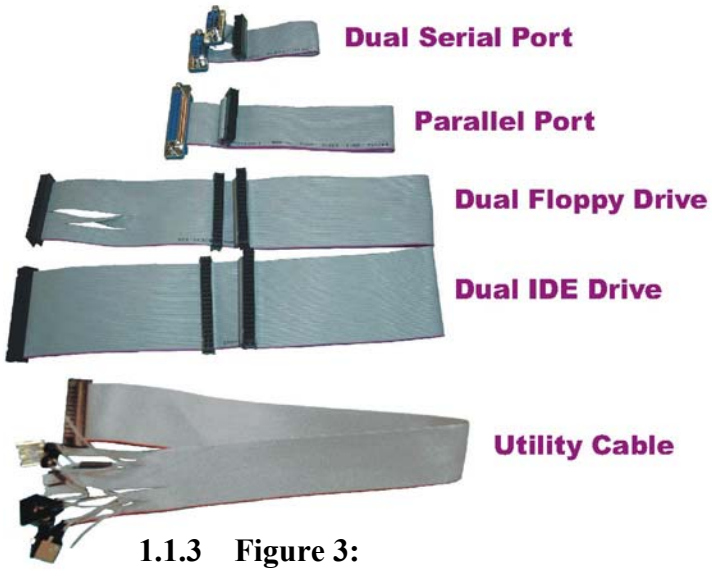
3.2 PIN-1 LOCATION



1.1.1 Figure 2: Pin-1

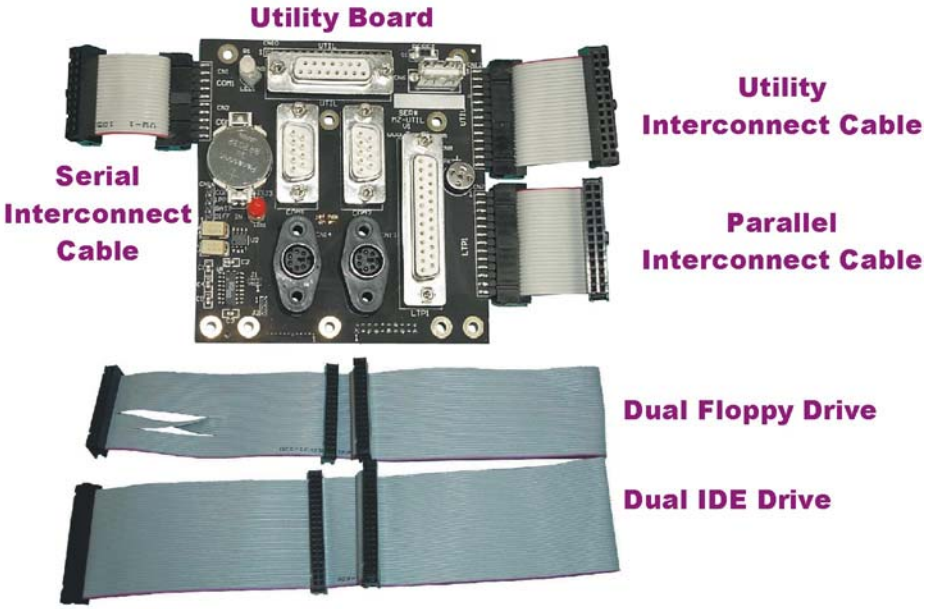
CHAPTER 4: TMZ104 CABLE SETS (OPTIONAL)

4.1 Cable set 1 (Part# CABLESET1-TMZ104)



1.1.3 Figure 3:
Cable Set 1

4.2 Cable set 2 (part# CABLeset2-TMZ104)



1.1.5 Figure 4:
Cable Set 2

CHAPTER 5: TMZ104 UTILITY BOARD (OPTIONAL)

The optional TMZ104 Utility Board, the UTIL104, provides a convenient means to connect peripheral devices to the TMZ104 embedded CPU module. It provides connectors to interface to standard PC peripherals. In addition, the UTIL104 provides some input/output functionality such as status LED and hardware-reset switch. For applications requiring a GPS receiver, the UTIL104 also acts as a carrier board to mate with several models of RoyalTek GPS receivers available from Tri-M Systems.

Figure 5: UTIL104 interfaced with a TMZ104

The TMZ104 Utility Board can be interfaced to the TMZ104 CPU module via three short flat ribbon cables provided with optional CABLESET2-TMZ104 (see figure 4) available from Tri-M Systems. The UTIL104 can be mounted above the TMZ104 with PC/104 stand offs.

		Connect Between	
Cable	Function	TMZ104	Utility Board
1" 20-pin (2x10) IDC ribbon cable	COM1/COM2	CN8/CN9	CN1/CN2
1" 26-pin (2x13) IDC ribbon cable	Parallel	CN5	CN7
1" 26-pin (2x13) IDC ribbon cable	Utility	CN7	CN12

Table 2: UTIL104 Interface

The UTIL104 utility board supports the Royaltek REB2000/2100 series as well as the REB12R series GPS receivers. A 12-position single-row female socket is provided for the REB2000/2100 series receiver while a 20-position dual-row female socket is provided for the REB12R series receiver. Power is provided to the UTIL104 board through connector CN7 on the TMZ104. No separate power source is required.

Note: J1 must be installed in order to route GPS output to CN3. Make sure to disconnect cable between CN1/CN2 and CN8 of TMZ104 to make COM1 and COM2 available.

CHAPTER 6: JUMPERS

Jumpers are provided on the TMZ104 to select the WDT input and the CPU core voltage of the System.

Jumpers	
Label	**Function**
JP1	WDT input select, internal or external
JP4	CPU core voltage 1.00 V or 1.15 V
JP5	DOC address or disabled

Table 3: List of Jumpers

6.1 WDT input select (JP1)

The WDT timeout counter can be reset internally through a GPIO pin of the Southbridge or externally through the utility connector. The dual mode watchdog timer provides a start up mode allowing lengthy boot to complete and a normal mode allowing quick system restart when the CPU activity fails.

During the normal operating mode, the supervisor will issue a reset pulse for the reset timeout period (140ms min) if the µP does not update the watchdog input with a valid transition (HIGH to LOW or LOW to HIGH) within the standard timeout period (1.6s minimum).

After each reset event (VCC power-up, manual reset, or watchdog reset), there is an initial watchdog start up timeout period of 25.6s minimum. The start up mode provides an extended period for the system to power up and fully initialize all µP and system components before assuming responsibility for routine watchdog updates. The normal watchdog timeout period (1.6s minimum) begins at the conclusion of the start up timeout period or after the first transition on the watchdog input before the conclusion of the start up period.

WDT	JP1
External trigger source	1-2
Internal trigger source	2-3
Disable	OFF

Table 4: WDT Select

6.2 CPU core voltage SELECT (JP4)

The TMZ104 was designed to be a very low power CPU board; therefore the CPU frequency was slowed down to run with a minimal core voltage. The jumper boosts the core voltage to allow the CPU frequency to increase if more CPU power is needed. This jumper must be ON to match the default OEM_CONFIG allowing the LongRun to set the CPU frequency up to 533MHz

CPU core voltage	Allowed CPU frequency	JP4
1.00 V	400 MHz & below	OFF
1.15V	Above 400 MHz	ON

Table 5: CPU Core Voltage Select

6.3 Diskonchip address SELECT (JP5)

The TMZ104 includes a socket to have the ability to use a solid-state disk "DiskOnChip" directly on the CPU board without additional hardware.

This jumper allows the user to select the memory address range of the DiskOnChip embedded on the CPU board or disable it.

DiskOnChip address	JP5
DISABLED	OFF
D0000 – D1FFF	3-4
D4000 – D5FFF	1-2

Table 5: DiskOnChip address Select

When detected the DiskOnChip is reported in the BIOS as a DiskOnChip or a SCSI card, depending of the DiskOnChip model and the firmware version. This information is shown under : BOOT → Hard Disk Drives.

CHAPTER 7: CONNECTORS

Connectors on the TMZ104 are provided to interface external devices such as a hard disk drive, floppy drive, and keyboard.

Table 7: TMZ104 Connector List

TMZ104 Connector List	
Connector Label	Function
CN4	External power connector
CN5	Parallel port connector
CN6	Floppy drive connector
CN7	Utility connector for keyboard, mouse, USB, battery and speaker
CN8	COM1 serial port connector
CN9	COM2 serial port connector
CN12	IDE drive connector
CN13	PC104 connector (40-pin)
CN14	PC104 connector (64-pin)
CN15	SO-DIMM memory socket
IC23	DiskOnChip socket

Note: Pin-1 of each connector on the TMZ104 is designated by a small, white dot on the PCB. Pin-1 of the connector should line up with pin-1 of the corresponding mating connector on the cable. Please refer to "Figure 2" for pin-1 location.

7.1 External Power (CN4)

The TMZ104 can be powered by supplying 5VDC and ground to CN4. Alternatively, the TMZ104 can be powered by supplying 5VDC through the PC104 connector (CN13) with a PC104 power supply such as the Tri-M Engineering HE104 or HESC-104.

Table 8: External Power Connector

External Power (CN4)	
Pin Number	**Signal**
1	Vcc +5V
2	GND

7.2 Interface (CN5)

The TMZ104 parallel port is fully compatible with the PC/AT parallel port. In the extended mode, it functions as a PS/2-like bi-directional port. In Extended Capabilities Port (ECP) mode, it is IEEE 1284 compliant, including level 2. The parallel ports uses the following PC resources when enabled:

Parallel Port	Typical Usage	I/O Address	Standard Interrupt
Parallel 1	LPT1	378H – 37Fh	IRQ7

Table 9: Parallel Port Resources

The default interrupt for parallel port LPT1 is IRQ7. The parallel port output signals provide up to 14mA drive current. RC filters are provided for noise suppression. The parallel port signals appear on CN5, a dual-row ribbon-cable pin edge connector. The port may be cabled to appear on a standard PC DB-25 connector. A DB-25 connector and cable are provided for this purpose in the optional TMZ104 cable kit. The following table shows the parallel port signals appearing on CN5 and the equivalent pinout on a DB-25 connector.

CN5	DB-25 Pin	Signal	Function	In/ Out	CN5	DB-25 Pin	Signal	Function	In/ Out
1	1	STRB -	Output data strobe	OUT	2	14	AUTOFD -	Auto feed	OUT
3	2	PD0	Data bit 0	I/O	4	15	ERR-	Printer error	IN
5	3	PD1	Data bit 1	I/O	6	16	INIT-	Initialize printer	OUT
7	4	PD2	Data bit 2	I/O	8	17	SLCTIN-	Selects printer	OUT
9	5	PD3	Data bit 3	I/O	10	18	GND	Signal Ground	N/A
11	6	PD4	Data bit 4	I/O	12	19	GND	Signal Ground	N/A
13	7	PD5	Data bit 5	I/O	14	20	GND	Signal Ground	N/A
15	8	PD6	Data bit 6	I/O	16	21	GND	Signal Ground	N/A
17	9	PD7	Data bit 7	I/O	18	22	GND	Signal Ground	N/A
19	10	ACK-	Character acknowledged	IN	20	23	GND	Signal Ground	N/A
21	11	BUSY	Printer busy	IN	22	24	GND	Signal Ground	N/A
23	12	PE	Out of paper	IN	24	25	GND	Signal Ground	N/A
25	13	SLCT	Printer selected	IN	26	N/A	GND	Signal Ground	N/A

Table 10: Parallel Port Connections

Note: CN5 is an edge mounted PCB connector with odd number pins located on the "top", and even number pins on the "bottom".

7.3 Floppy Interface (CN6)

The floppy interface provides the signal to control two 3 ½" and/or 5 ¼" floppy drives. A 34-pin daisy-chain drive connector cable is required for a dual-drive system. The default interrupt request for the floppy interface is IRQ6.

Pin	Signal	Pin	Signal
1~33 (odd)	GND	2	High Density Drv0
4	Unused	6	High Density Drv1
8	Index	10	Motor Enable
12	Drive Select B	14	Drive Select A
16	Motor Enable B	18	Direction
20	Step Pulse	22	Write Data
24	Write Enable	26	Track 0
28	Write Protect	30	Read Data
32	Select Protect	34	Disk Change

Table 11: Floppy Interface

7.4 Utility Port (CN7)

The utility connector provides the following inputs and outputs:

- Keyboard
- PS/2 mouse
- Universal Serial Bus
- Infrared port
- Speaker
- CMOS backup battery
- Watchdog trigger source
- Hardware reset
- Hard drive LED

Signals on CN7 can be terminated using the optional TMZ104 utility board, the UTIL104. The UTIL104 provides the appropriate connectors for all the signals.

Utility Connector (CN7)		
Pin	**Signal**	**Function**
1	KBDATA	Keyboard data
2	KBCLK	Keyboard clock
3	MDATA	P/S 2 mouse data
4	MCLK	P/S2 mouse clock
5	KBLOCK	Keyboard lock
6	SPKOUT	Speaker output
7, 8	GND	Ground
9, 10	KBMPWR	+5V
11	NC	No connection
12	WDEXT	External trigger source for watchdog timer
13	IRTx	Infrared transmit
14	IRRx	Infrared receive
15	RESET	Hardware reset
16	HDDLEDOUT	Hard drive LED output (8mA source)
17	NC	No connection
18	NC	No connection
19	VCC-EXTBAT	RTC Backup battery +V terminal (3.6V)
20	GND	Ground
21	SCL	SMBus clock
22	SDA	SMBus data
23	USBVCC1	USB port 1 power
24	USBD1F-	USB port 1 data minus
25	USBD1F+	USB port 1 data plus
26	USBGND1	USB port 1 ground

Table 12: Utility Connector

7.5 SERIAL INTERFACES (CN8, CN9)

The TMZ104 provides two PC-compatible asynchronous serial ports. Typically, DOS and Windows treat the serial ports as COM1, and COM2. Standard system resources are allocated to the serial ports:

Serial Port	Typical Usage	I/O Address	Standard Interrupt
Serial 1 (CN8)	COM1	3F8h–3FFh	IRQ4
Serial 2 (CN9)	COM2	2F8h–2FFh	IRQ3

Table 13: Serial Port Resources

Serial 1 and Serial 2 ports can be disabled using BIOS SETUP. When disabled, the port's I/O address is made available for other expansion devices on the 16-bit BUS.

A full complement of input and output handshaking lines is supplied by serial port COM1 and COM2. These signals are at standard RS232C levels. The RS232C level converters provide the required RS232C voltage levels with internal +5 volt to ±9 volt converters.

CN 8	DB-9 Pin	Signal	Function	In/ Out	CN8	DB-9 Pin	Signal	Function	In/ Out
1	1	DCD1	Serial 1 Data Carrier Detect	IN	2	6	DSR1	Serial 1 Data Set Ready	IN
3	2	RXD1	Serial 1 Receive Data	IN	4	7	RTS1	Serial 1 Request To Send	OUT
5	3	TXD1	Serial 1 Transmit Data	OUT	6	8	CTS1	Serial 1 Clear To Send	IN
7	4	DTR1	Serial 1 Data Terminal Ready	OUT	8	9	RI1	Serial 1 Ring Indicator	IN
9	5	GND	Signal Ground		10		N/C	No connection	

Table 14: Serial Port COM1 Connection

CN 9	DB-9 Pin	Signal	Function	In/ Out	CN9	DB-9 Pin	Signal	Function	In/ Out
1	1	DCD1	Serial 1 Data Carrier Detect	IN	2	6	DSR1	Serial 1 Data Set Ready	IN
3	2	RXD1	Serial 1 Receive Data	IN	4	7	RTS1	Serial 1 Request To Send	OUT
5	3	TXD1	Serial 1 Transmit Data	OUT	6	8	CTS1	Serial 1 Clear To Send	IN
7	4	DTR1	Serial 1 Data Terminal Ready	OUT	8	9	RI1	Serial 1 Ring Indicator	IN
9	5	GND	Signal Ground		10		N/C	No connection	

Table 15: Serial Port COM2 Connection

Note: CN8 and CN9 are an edge mounted PCB connector with odd number pins located on the "top", and even number pins on the "bottom". Pin-1 is designated by a white dot on the PCB.

7.6 IDE Interface (CN12)

The TMZ104 has a PCI bus mastering ATA-4 compatible IDE controller. The IDE controller supports Ultra DMA, Multi-word DMA, and all Programmed I/O (PIO) modes. Up to two drives can be connected, in a master-slave arrangement. Generally, the first hard disk drive (master) will appear as the C drive to DOS. The second drive, if attached, will appear as D.

Resource	Function
I/O Address (1F0h-1F7h)	Hard Disk Interface
IRQ14	Interrupt

Table 16: Hard Disk Resources

The Bios automatically detects all the IDE devices connected to the CPU board when the IDE controller is enabled in the BIOS setting (default). The user still able to configure everything manually through the BIOS setup.

IDE Interface (CN12)							
Pin	Signal Name	Function	In/Out	Pin	Signal Name	Function	In/Out
1	HDRESET-	Reset signal from host	OUT	2	GND	Ground	
3	HDD07	Data bit 7	I/O	4	HDD08	Data bit 8	I/O
5	HDD06	Data bit 6	I/O	6	HDD09	Data bit 9	I/O
7	HDD05	Data bit 5	I/O	8	HDD10	Data bit 10	I/O
9	HDD04	Data bit 4	I/O	10	HDD11	Data bit 11	I/O
11	HDD03	Data bit 3	I/O	12	HDD12	Data bit 12	I/O
13	HDD02	Data bit 2	I/O	14	HDD13	Data bit 13	I/O
15	HDD01	Data bit 1	I/O	16	HDD14	Data bit 14	I/O
17	HDD00	Data bit 0	I/O	18	HDD15	Data bit 15	I/O
19	GND	Ground		20	KEY	Keyed pin	N/C
21	IDEPDREQ	DMA 0 Request	OUT	22	GND	Ground	
23	HDIOW-	Write strobe	OUT	24	GND	Ground	
25	HDIOR-	Read strobe	OUT	26	GND	Ground	
27	HDRDY	I/O Channel Ready	IN	28	GND	Ground	
29	IDEPDACK	DMA 0 Acknowledge	IN	30	GND	Ground	
31	IRQ14	Drive interrupt request	IN	32	IOCS16-	I/O Chip Select 16	In
33	HDA1	IDE Address 1	Out	34	RSVD	Reserved	N/C
35	HDA0	IDE Address 1	Out	36	HDA2	IDE Address 2	Out
37	HDCS0-	IDE Chip Select 0	Out	38	HDCS1-	IDE Chip Select 1	Out
39	LEDIN-			40	GND	Ground	

Table 17: IDE Drive Interface

NOTE: For maximum reliability, IDE drive cables should be limited to 18 inches or less in length.

7.7 PC/104 connector (CN14 and CN13)

Both CN13 and CN14 provide the flexibility to attach PC/104 expansion modules to the TMZ104. These modules perform the functions of traditional add-in cards in a PC environment. All data, address and control signals are able to sink 10mA and source 8mA.

PC/104 8-bit Connector (CN14)			
Pin #	**Signal**	**Pin #**	**Signal**
A1	/IOCHCK	B1	GND
A2	SD7	B2	RESETDRV
A3	SD6	B3	+5V
A4	SD5	B4	IRQ9
A5	SD4	B5	-5V
A6	SD3	B6	DRQ2
A7	SD2	B7	-12V
A8	SD1	B8	/0WS
A9	SD0	B9	+12V
A10	IOCHRDY	B10	GND(*)
A11	AEN	B11	/SMEMW
A12	SA19	B12	/SMEMR
A13	SA18	B13	/IOW
A14	SA17	B14	/IOR
A15	SA16	B15	/DACK3
A16	SA15	B16	DRQ3
A17	SA14	B17	/DACK1
A18	SA13	B18	DRQ1
A19	SA12	B19	/REFRESH
A20	SA11	B20	SYSCLK
A21	SA10	B21	IRQ7
A22	SA9	B22	N/A
A23	SA8	B23	IRQ5
A24	SA7	B24	IRQ4
A25	SA6	B25	IRQ3
A26	SA5	B26	/DACK2
A27	SA4	B27	TC
A28	SA3	B28	BALE
A29	SA2	B29	+5V
A30	SA1	B30	OSC
A31	SA0	B31	GND
A32	GND	B32	GND

Table 18: PC/104 8-bit Interface

PC/104 16-bit Connector (CN13)			
Pin #	**Signal**	**Pin #**	**Signal**
C0	GND	D0	GND
C1	/SBHE	D1	/MEMCS16
C2	LA23	D2	/IOCS16
C3	LA22	D3	IRQ10
C4	LA21	D4	IRQ11
C5	LA20	D5	IRQ12
C6	LA19	D6	IRQ15
C7	LA18	D7	IRQ14
C8	LA17	D8	/DACK0
C9	/MEMR	D9	DRQ0
C10	/MEMW	D10	/DACK5
C11	SD8	D11	DRQ5
C12	SD9	D12	/DACK6
C13	SD10	D13	DRQ6
C14	SD11	D14	/DACK7
C15	SD12	D15	DRQ7
C16	SD13	D16	+5V
C17	SD14	D17	/MASTER
C18	SD15	D18	GND
C19	GND(*)	D19	GND

Table 19: PC/104 16bit Interface

7.8 SO-DIMM Socket (CN15)

The SO-DIMM memory socket accommodates one 144-pin SO-DIMM memory module. The SO-DIMM connector on the TMZ104 is "wired" as a dual slot with one bank on each slot. The memory used on the TZM104 must be compatible with this architecture. The memory supplied by Tri-M Engineering for the TMZ104 is a "standard" SO-DIMM pcb with the two memory banks populated as required. The memory is a 64-bit, 3.3V PC100 or PC133 SDRAM that needs 32MB 4Mbx16bits on the "bottom" of the SO-DIMM. The TMZ104 supports a maximum of 256MB user upgradable SDRAM, not including the 32MB on the bottom of the SO-DIMM. For further information on TMZ104 Memory, please refer to Appendix 1 of this manual.

TMZ104 SDRAM SO-DIMM modules (*****) are available from Tri-M Systems.

Part number: MEM-32+XX-TMZ (XX = capacity extension in MB)

Examples:

MEM-32+0-TMZ: A 32MB module with 16MB available for user applications (16MB reserved for Code Morphing software).
MEM-32+128-TMZ: User upgrade memory of 128MB for a total of 144MB for user applications (16MB reserved for Code Morphing software).

7.9 DiskOnChip Socket (IC23)

The TMZ104 provides a 32-pin DIP socket, which can be populated with an M-Systems' DiskOnChip 2000 or a DiskOnChip Millennium product.

Pin Name	Description	Pin Number	Direction
A0 – A12	Address bus	4-12, 23, 25-27	Inputs
D0 – D7	Data bus	13-15, 17-21	I/O
CE/	Chip Enable	22	Input
OE/	Output Enable	24	Input
WE/	Write Enable	31	Input
NC	Not Connected	1, 2, 3, 28, 29, 30	
VCC	Power	32	
GND	Ground	16	

Table 21: DiskOnChip Socket (IC23)

CHAPTER 8: SETUP

8.1 TMZ104 Interrupt AND I/O Port assignments

IRQ Number	TMZ104 Assignment
0	Systems timer (not available for other devices)
1	Keyboard controller (not available for other devices)
2	Second PIC cascade (not available for other devices)
3	Serial port two (COM2:)
4	Serial port one (COM1:)
5	Unassigned
6	Floppy Disk controller (not available for other devices)
7	Parallel (printer) port one (LPT1:)
8	Real-time clock (RTC)
9	Unassigned
10	Unassigned
11	USB
12	PS/2 Mouse
13	Math coprocessor
14	Primary IDE
15	unassigned

Table 22: TMZ104 Interrupt Assignments

I/O Address	Hardware
0000 - 000F	DMA Controller
0020 – 0021	PIC
0022 – 0021	Motherboard Resources
0040 – 0043	System Timer
0060 – 0060	Keyboard
0061 – 0061	Systems Speaker
0064 – 0064	Keyboard
0070 – 0071	System CMOS / Real time clock
0081 - 008F	DMA Controller
0092 – 0092	Motherboard Resources
00A0 - 00A1	PIC
00C0 - 00DF	DMA Controller
00F0 - 00FF	Numeric Data Processor
02F8 - 02FF	Communications Port B
0378 - 037F	Printer Port
03F0 - 03F5	Floppy Disk Controller
03F7 - 03F7	Floppy Disk Controller
03F8 - 03FF	Communications Port A
0480 - 048F	Motherboard Resources
04D0 - 04D1	Motherboard Resources
0778 - 077F	Printer Port
0CF8 - 0CFF	PCI Bus
AC00 - AC1F	Motherboard Resources
AC80 - AC9F	Motherboard Resources

Table 23: TMZ104 I/O Port Assignments

8.2 BIOS Setup

The TMZ104 system BIOS (Basic Input Output System) supports a standard SETUP function to configure system parameters. The BIOS uses these parameters to establish default conditions during system initialization, both during the Power On Self Test (POST) phase, and during system boot.

8.3 Using SETUP

To enter the SETUP function, press the <DEL> key during POST.

Note: When you change SETUP parameters, the new values do not take effect until the system is rebooted.

CHAPTER 9: LONGRUN™

The LongRun is enabled by default on the TMZ104 allowing the CPU to switch its frequency on the fly depending of the CPU workload.

The following frequencies are programmed by default in the TMZ104 OEM CONFIG:

Frequency	VCORE required	SDRAM divider	SDRAM Speed	PCI divider
200 Mhz	0.90V	3	66Mhz	6
266 Mhz	0.90V	3	89Mhz	8
333 Mhz	0.95V	3	111Mhz	10
400 Mhz	1.00V	4	100Mhz	12
466 Mhz	1.05V	4	116Mhz	14
533 Mhz	1.10V	5	106Mhz	16
600 Mhz	1.15V	5	120Mhz	18
667 Mhz	1.20V	6	111Mhz	20

The longRun is configured by default with the lower boundary at 333MHz and the upper boundary at 533MHz, allowing the CPU to switch automatically between 333MHz, 400Mhz, 466MHz and 533Mhz.
The others frequencies are for experimental use only and are not warranty by the manufacturer.

Power consumption measurements of a TMZ104 CPU board with 32MB SDRAM and 8MB Diskonchip for low workload and full CPU load.

Frequency	VCORE 1V	VCORE 1.15V	VCORE 1V	VCORE 1.15V
200 Mhz	1.72W	1.79W	2.35W	2.67W
266 Mhz	1.70W	1.78W	2.54W	2.95W
333 Mhz	1.80W	1.89W	2.82W	3.33W
400 Mhz	1.88W	1.97W	3.26W	3.70W
466 Mhz	1.86W	1.98W	3.11W	3.96W
533 Mhz	1.93W	2.04W	3.53W	4.31W
600 Mhz	1.91W	2.03W	3.70W	4.60W
667 Mhz	1.96W	2.09W	4.00W	4.98W
	Linux kernel 2.4.18 + Bash shell	**Linux kernel 2.4.18 + Bash shell**	**Linux kernel 2.4.18 + cpuburn**	**Linux kernel 2.4.18 + cpuburn**

Note: The following power consumption measurement was made with the CPU frequency fixed, Upper boundary = Lower boundary disabling the LongRun feature

CHAPTER 10: WATCHDOG

10.1 External (JP1 1-2)

The watchdog is enabled with external timer reset when JP1 is set on position 1-2 and a level high or low is applied to pin 12 of the utility connector. A reset will be issued at the end of a fixed delay, typically 46.4s (minimum 25.6s) after power-on or reset event and 2.9s (minimum 1.6s).

The external circuitry has to toggle (high to low or low to high) the utility pin-12 input before the delay expires to avoid the system to be reset.

10.2 Internal (JP1 2-3)

The watchdog is enabled with internal timer reset when JP1 is set on position 2-3. A reset will be issued at the end of the fixed delay, typically 46.4s (minimum 25.6s) after power on or reset event and 2.9s (minimum 1.6s).

The programming of the GPIOA pin of the Southbridge will need to be updated before the delay expires to avoid a system reset.

The GPIOA is programmed through the PCI registers of the Southbridge. The General Purpose I/O registers are offset 70h to 77h of the Function 0, and are used to configure the GPIO pins of the Southbridge. The IO Space needs to be initialized to be able to program the GPIO pins. The IO Space can be configured through the PCI registers Function 4 offset 48h-49h. The GPIO pins are programmed through the IO Space offset 48h-4Fh.

The GPIOA is control the Watchdog:

- The pin can be defined as a GPIOA through Function 0 Offset 76h bit 0.
  0 = pin defined as GPIOA; 1 = pin defined as GPOWE.

- The pin can be defined as an OUTPUT through Function 0 Offset 74h bit 2.
  0 = INPUT; 1 = OUTPUT.

- The IO Space can be configured through Function 4 Offset 48h and 49h.
  49h-48h: 15 – 7 I/O BASE

- The GPIOA pin can be programmed through the IO Space base address + offset 4Ch to4Fh
  4Fh-4Ch : 31 – 26 Reserved
  25 – 0 GPO

More information is available in the VIA VT82C686B Super Southbridge datasheet.

TMZ104 MEMORY INFORMATION

The processor on the TMZ104 requires SDRAM (Synchronous Dynamic Random Access Memory) as "main memory". This memory is composed of two independent banks of memory. The base memory of 32MB, using four chips of 4M by 16 bits, on the bottom of the SO-DIMM module and the extension (or field upgradable) memory on the top of the SO-DIMM the module. This extension memory must be populated with four 16 bits memory chips or not installed. The base memory of 32MB is statically configured to be able to start the Code Morphing Software and can not be changed. The Code Morphing Software reserves 16MB of the base memory to load and execute itself, therefore that part of the memory is locked and is not available for user applications. The remaining 16MB can be used for user applications. The BIOS automatically detects the amount of extension memory installed in the system and reports the maximum available memory for user applications (the addition of the remaining 16MB of the base memory and the extension memory).

The main memory of the TMZ104 must be compatible to the Tri-M Engineering uses a modular memory approach with the TMZ104, thus allowing customers to select the size of memory that best fits their application.

The following SO-DIMM memory modules are available:

1.2.1 Part Number	Total Memory size	User Application Memory available
MEM-32+0-TMZ	32MB	16MB
MEM-32+32-TMZ	64MB	48MB
MEM-32+64-TMZ	96MB	80MB
MEM-32+128-TMZ	160MB	144MB

Detailed memory modules composition:

1.2.2 Part Number	Total Memory size	Top side	Bottom side
MEM-32+0-TMZ	32MB	empty	4chips of 4M x 16 bits
MEM-32+32-TMZ	64MB	4chips of 4M x 16 bits	4chips of 4M x 16 bits
MEM-32+64-TMZ	96MB	4chips of 8M x 16 bits	4chips of 4M x 16 bits
MEM-32+128-TMZ	160MB	4chips of 16M x 16 bits	4chips of 4M x 16 bits

The Tri-M memory modules are populated with the following memory chips:

Chips 4M x 16 bits are: SAMSUNG K4S641632E-TC80
Chips 8M x 16 bits are: MICRON 48LC8M16A2-75 B
Chips 16M x 16 bits are: MICRON 48LC16M16A2-75 C

2 LONGRUN™ MSR REGISTERS

When LongRun is enabled (as it is by default on the TMZ104) the MSR registers can be query to have information about the present status and can be used to modify some parameters of the actual setting.

CPUID Processor Info

Index	Registers	information
8086:0001h	EAX	Processor identification
	EBX	Processor revision
	ECX	Processor core frequency
	EDX	Processor enabled features

CPUID LongRun Status

Index	Registers	information
8086:0007h	EAX	Current processor core frequency
	EBX	Current processor core voltage
	ECX	Current performance percentage
	EDX	Reserved

MSR LongRun Control and Status

Index	Registers	information
8086:8010h	EAX	Lower boundary of the performance window, in percent (%)
	EDX	Upper boundary of the performance window, in percent (%)

MSR LongRun Flags

Index	Registers	information
8086:8011h	EAX	Bit 0 indicate the LongRun mode: 0 = performance, 1 = economy
	EDX	Reserved

MSR LongRun Table Readout

Index	Registers	information
8086:8018h	EAX	Currently shown level number
	EDX	Maximum level number

MSR LongRun Level Index

Index	Registers	information
8086:8019h	EAX	Performance index for this level
	EDX	Reserved

MSR LongRun Frequency and Voltage

Index	Registers	information
8086:801Ah	EAX	Frequency in MHz
	EDX	Voltage in mV

MSR LongRun Memory Divisors

Index	Registers	information
8086:8019h	EAX	SD RAM frequency divisor
	EDX	DDR RAM frequency divisor

MSR LongRun I/O Divisors

Index	Registers	information
8086:801Ah	EAX	PCI divisor
	EDX	Reserved

MSR LongRun Gate Delay

Index	Registers	information
8086:801Ah	EAX	Measured gate delay
	EDX	Reserved

More information about the Crusoe MSR registers is available on the Transmeta web site.
http://www.transmeta.com/developers/techdocs.html

3 LITERATURE REFERENCES

The following references are for information about the PC/104 architecture, the PC DOS, and the PC BIOS.

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MindShare, Inc., Tom Shanley and Don Anderson
Internet: mindshar@interserv.com
CompuServe: 72507,1054
Published by Addison Wesley, Inc.

30.2 AT Bus Design

Edward Solari
Anabooks
12145 Alta Carmel Ct., Suite 250
San Diego, CA 92128
ISBN 0-929392-08-6

30.3 Personal Computer Bus Standard P996

Institute of Electrical and Electronic Engineers, Inc.
445 Hoes Lane
Piscataway, NJ 08854

30.4 PC Interrupts

PC Interrupts, Ralf Brown, Addison/Wesley.

30.5 BIOS Reference

System BIOS for IBM PC/XT/AT Computers, Phoenix, Addison/Wesley

30.6 PC/104 Consortium

809 B-175 Cuesta Drive,
Mountain View, CA 94040
Phone: 415 903-8304
FAX: 415 967-0995

30.7 DiskOnChip

M-Systems Corp
8371 Central Avenue Suite A
Newark, CA 94560
Phone: 510-494-2090
FAX: 510-494-5545