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MZ104+

user manual V3.0

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WARNING

- A working knowledge of electronics and PC-technology is required to use this product.
- Pay attention to electrostatic discharges. Use a CMOS protected workplace.
- Disconnect power source when connecting any cables or devices.

**This is a high-technology product.
A working knowledge of electronics and
PC-technology is required!**

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CHAPTER 1 – GENERAL INFORMATION

1.1 GENERAL DESCRIPTION

The MZ104+ embedded control module incorporates the revolutionary ZFx86™ “PC-on-a-chip” processor with dual 10/100BaseT Ethernet and 32-bit PCI Bus. The MZ104+ offers the quickest route of integrating a full x86 AT-compatible computer into your embedded control application using the PC/104+ form factor. The MZ104+ is fully compatible with all standard PC Software and will run any standard operating system capable of running on a fully compatible PC with FPU such as Linux, DOS, many RTOS, and WinCE, Windows 9x, and Windows NT.

1.2 SPECIFICATIONS

586 CPU

- 32-bit CPU core operating at 133¹, 128, 100, 66, 64 and 33MHz
- 8K byte Level 1 cache, write back and write through support
- Floating point unit

PC Core Logic with PCI enhancement

- 32 bit 33MHz PCI rev 2.1 compliant “Northbridge” and “Southbridge”
- AT-compatible DMA controllers, interrupt controllers, timer/counters
- AT keyboard controller and Real-time clock

Memory

- Synchronous DRAM support
- Onboard 144-pin DIMM socket for up to 64MB SDRAM

Ethernet Interface

- Dual Intel 82559ER 10/100 BaseT Fast Ethernet Controllers.

FDD interface

- Supports one floppy disk drive

Enhanced IDE Interface

- One enhanced IDE channel, supports up to two drives (master/slave)
- PCI bus master burst reads and writes
- Ultra DMA and PIO modes (1-4) support

Serial Ports

- Two 16550-compatible RS232 serial ports
- Baud rates up to 115.2 K baud

Parallel Ports

- One enhanced bi-directional parallel port
- Supports SPP, ECP and EPP

Universal Serial Bus

- Dual USB ports. USB 1.1 and OpenHCL compliant
- PCI bus master burst reads and writes
- Over current and power control support

Keyboard/Mouse Interface

- Supports AT keyboard and PS/2 mouse

¹ 133MHz is overclocking. Additional cooling is required.

Power Management

- I/O traps and idle timers for peripheral power management
- Hardware and software CPU suspend mode support

Solid State Flash Storage

- One 32-pin DIP socket supports M-Systems DiskOnChip 2000 and DiskOnChip Millennium
- 8 – 288 MB Capacity

Expansion Bus

- Fully Compliant 16-bit PC/104 Expansion BUS
- Fully Compliant 32-bit PC/104+ Expansion BUS

Electrical Specifications

- Support for low-power modes via BIOS APM features

		MEMORY SIZE			
		8 MB	16 MB	32 MB	64 MB
SPEED	33 MHz	804 mA	808 mA	806 mA	833 mA
	66 MHz	863mA	868 mA	866 mA	893 mA
	100 MHz	925 mA	930 mA	928 mA	940 mA

Table 1: MZ104+ Power Consumption

Note: Power consumption figure is averaged with APM disabled.

Mechanical/Environmental

- PC/104+ form factor compliant, 3.55" x 3.775 x 0.9" (90mm x 96mm x 23mm)
- Standard PC/104+ 32-bit stackthrough connector for PC/104+-compliant modules
- ZFx86 Case Temperature (33, 66, 100MHz operation): -40° to 185°F (-40° to 85°C)²
- ZFx86 Case Temperature (133MHz operation): -4° to 158F (-20° to 70C)
- Storage temperature: -67° to 185°F (-55° to 85°C)
- Weight: 0.15 lb. (70 g)

² Extended temperature memory available upon request.

1.3 EMBEDDED FEATURES

FailSafe Boot ROM

- 12Kbyte BIOS update ROM (BUR) to allow flash BIOS install or upgrade
- Provides permanent and fail-safe mechanism to update software under all adverse conditions
- External Fail-Safe™ Code may be installed in optional 8 – 32Kb SEEPROM inserted into socket IC1

Z-Tag Interface

- High speed interface to download software
- Uses floppy interface when “Drive Select” signal is inactive
- Communication protocol compatible with serial EEPROMs
- Z-tag programming tool allows easy field upgrade

Dual Watchdog Timer

- Software and hardware control of WatchDog Timer event
- 16 bit counter primary watch dog connected to WSIRQ/NMI/SMI, reset by WDT input
- Second 8 bit counter connect to H/W reset line, enabled by primary counter output

Software included

- Phoenix embedded PC BIOS – 100% X86 compatible

Software Compatibility

- Linux
- MSDOS 3.X, 4.X, 5.X, 6.X, DRDOS
- Win95/98/NT
- Most PC-Compatible RTOS
- WindRiver VxWorks RTOS

CHAPTER 2 - INSTALLATION

2.1 LOCATING THE CONNECTORS & JUMPERS

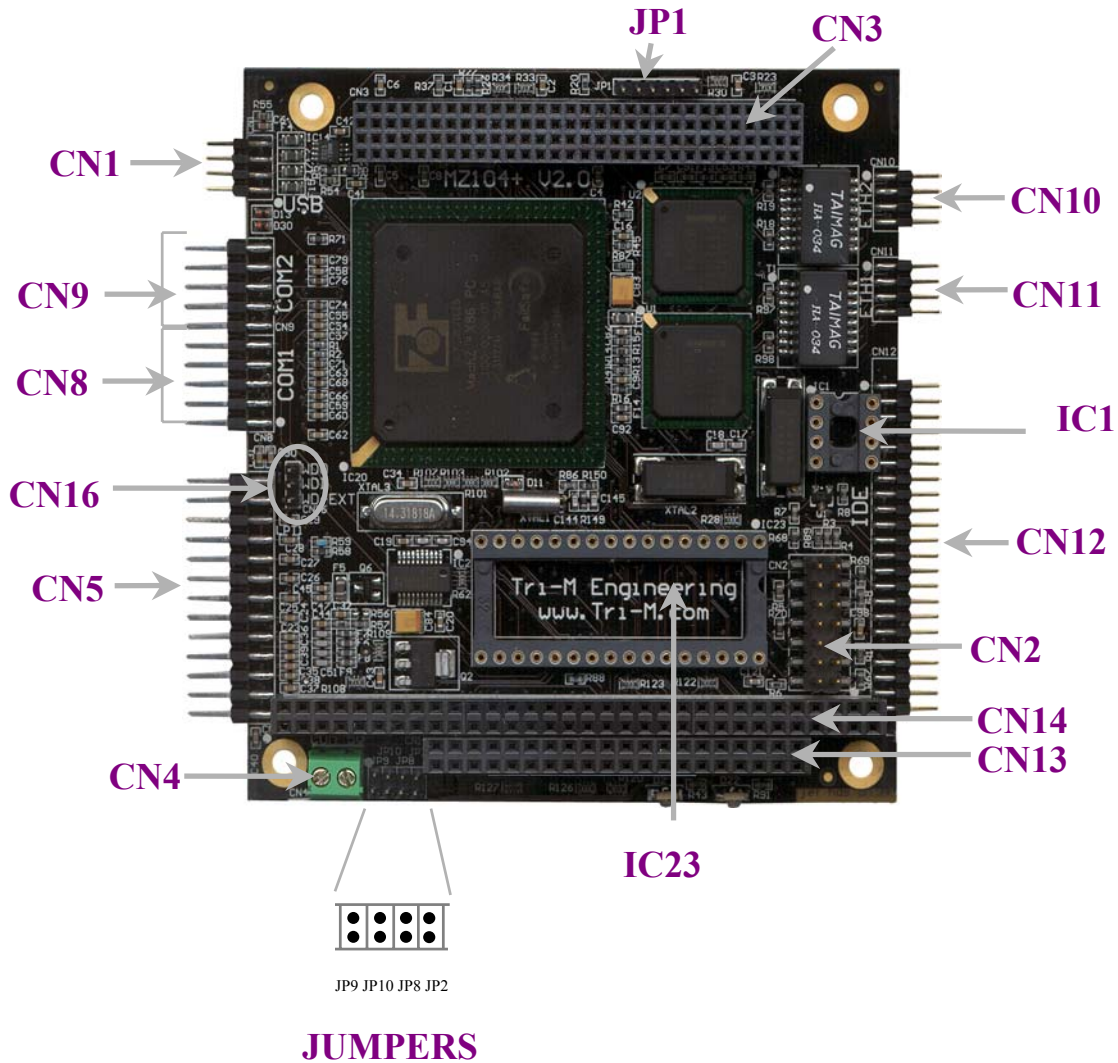


Figure 2: Connector and Jumper location MZ104+ top

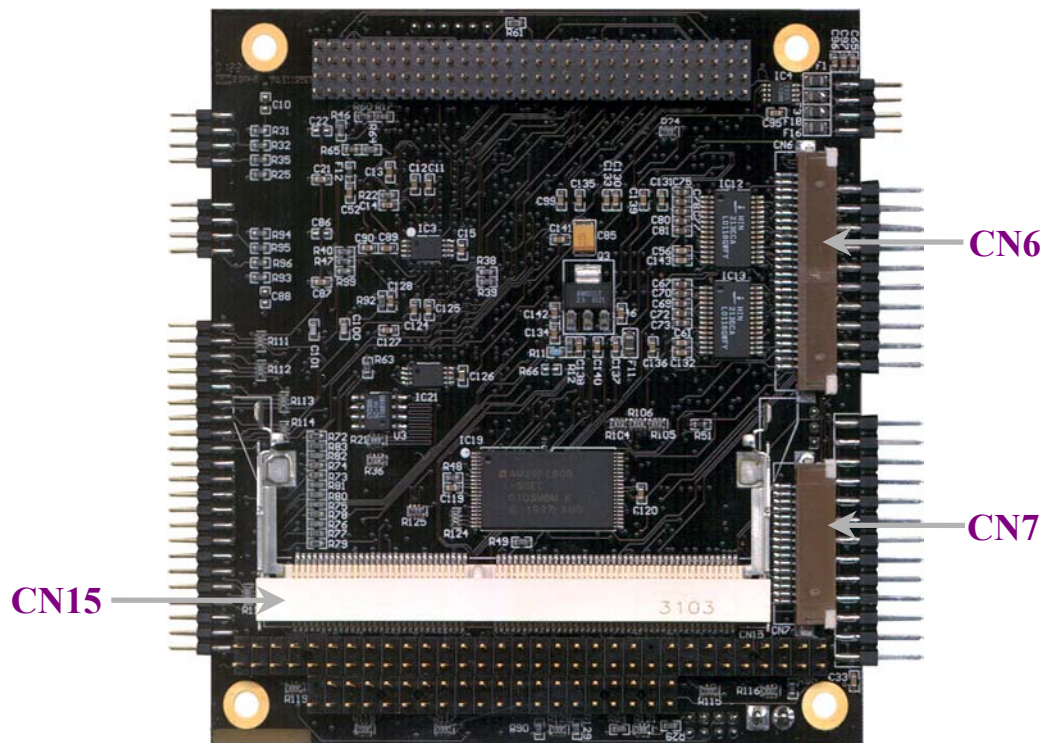


Figure 3: Connector and Jumper location MZ104+ bottom.

2.2 OPTIONAL MZ104+ UTILITY BOARD (UTIL104+)

The MZ104+ Utility Board, the UTIL104+ (see Figure 4) provides a convenient means to connect peripheral devices to the MZ104+ embedded CPU module. In addition, the UTIL104+ provides some input/output functionality such as a status LED, hardware-reset switch. For applications requiring a GPS receiver, the Utility Board also acts as carrier board to mate with several models of Royaltek GPS receivers available from Tri-M Systems.

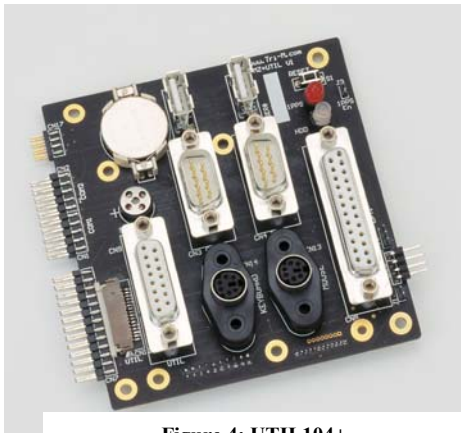


Figure 4: UTIL104+

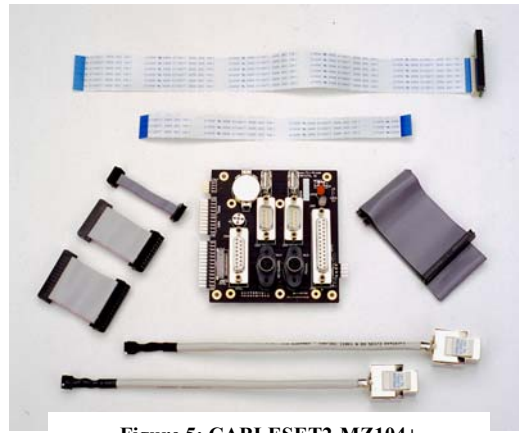


Figure 5: CABLESET2-MZ104+

The UTIL104+ interfaces to the MZ104+ CPU module via the three, 2" ribbon cables and one, 8" flex-foil cable provided with the optional CABLESET2-MZ104+ available from Tri-M. The UTIL104+ can be mounted above the MZ104+ with PC/104 stand offs.

Cable	Function	Connect Between	
		MZ104+	Utility Board
2" 8-pin (2x4) IDC ribbon cable	USB	CN1	CN17
2" 20-pin (2x10) IDC ribbon cable	COM1/COM2	CN8/CN9	CN1/CN2
2" 26-pin (2x13) IDC ribbon cable	Parallel	CN5	CN7
8" 16-pin flex-foil cable	Utility	CN7	CN12

Table 2: UTIL104+ Interface

The UTIL104+ supports the Royaltek REB2000/2100 series as well as the REB12R series GPS receivers. A 12-position single-row female socket is provided for REB2000 series receiver while a 20-position dual-row female socket is provided for REB12R series receiver. Power is provided to the UTIL104+ board through connector CN7 on the MZ104+. No separate power source is required.

Note: If J1 is ON, the GPS receiver uses COM1 of the MZ104+ CPU module exclusively for communication to the host. Therefore, COM2 is the only port available on the MZ104+ for communication to the GPS receiver.

CHAPTER 3 - JUMPERS

Jumpers are provided on the MZ104+ to enable/disable the PC/104+ Bus, select the BUR/Boot ROM, and set the CPU clock speed.

Jumpers	
Label	Function
JP1	PC104+ Bus mastering enable/disable
JP2	PC/104+ Bus enable/disable
JP3, JP4, JP5	System clock select
JP6	CPU core voltage select
JP8	BUR/Boot ROM select
JP9, JP10	Clock multiplier select
CN16	Watchdog select
CN18	Z-tag LED/Reset select

Table 3: List of Jumpers

3.1 PC104+ BUS MASTERING ENABLE/DISABLE (JP1)

JP1 enables/disables Bus mastering signals to the third PCI slot on the MZ104+ PC104+ Bus. If Bus mastering is **ENABLED**, the ISA Bus signals DACK1/DRQ1 are not available while GNT2/REQ2 on the PCI Bus are available. Conversely, if Bus mastering is **DISABLED**, the signals DACK1/DRQ1 on the ISA Bus are available while the PCI Bus signals GNT2/REQ2 are not available. The factory setting on the MZ104+ is Bus Mastering **ENABLED**.

PC/104+ Bus Mastering Enable/Disable (JP1)	
Pin	Function
1	Dack1X
2	Dack_1x
3	PGNT2X
4	DRQ1
5	DRQ_1
6	PREQ2X

Table 4: PC/104+ Bus Mastering Enable/Disable

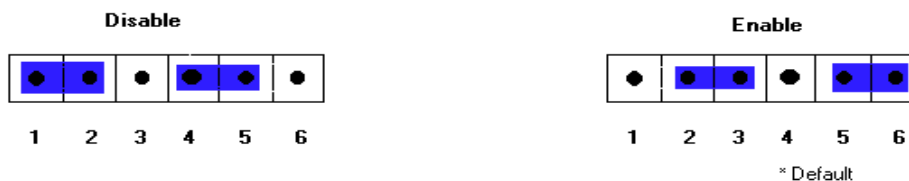


Figure 4: PC/104+ Bus Mastering Jumper Positions

3.2 PC/104+ BUS ENABLE/DISABLE (JP2)

JP2 allows the user to enable or disable the 32-bit PC/104+ Bus connector (CN3) on the MZ104+. If JP2 is unpopulated, the PC/104+ Bus connector is disabled. Populating the JP2 jumper enables the PC/104+ Bus.

3.3 SYSTEM CLOCK SELECT (JP3, JP4, JP5)

JP3, JP4 and JP5 allow the user to select the main system clock. JP5 also enable or disable the Frontside PCI clock divider if the system clock is higher than 33 MHz.

JP3	JP4	JP5	System Clock	Frontside PCI Clock
OFF	OFF	1-2	64 MHz	32 MHz
OFF	OFF	2-3	33 MHz	33 MHz
OFF	ON	1-2	66 MHz*	33 MHz*
OFF	ON	2-3	25 MHz	25 MHz
ON	OFF	1-2	50 MHz	25 MHz
ON	OFF	2-3	16 MHz	16 MHz
ON	ON	1-2	40 MHz	20 MHz
ON	ON	2-3	8 MHz	8 MHz

Table 5: SYSTEM CLOCK Select

* Factory Setting

3.4 CPU CORE VOLTAGE SELECT (JP6)

JP6 allows the user to select the core voltage of the CPU to work in higher frequency. The normal core voltage is 2.5 V but need to be increase to 2.7 V when the CPU clock is higher than 100 MHz.

CPU CORE VOLTAGE select (JP6)		
JP6	2.7 Volt OFF	2.5 Volt* ON

Table 6: BUR/BOOT ROM Select

* Factory Setting

3.5 BUR/BOOT ROM SELECT (JP8)

JP8 allows the MZ104+ to boot from standard BIOS or BUR. If boot ROM mode is selected, the MZ104+ will startup normally by executing the BIOS code and transfer control to a boot device. If BUR mode is selected, the MZ104+ will execute the BUR code to update the flash BIOS using the Z-Tag interface. It also provides an elementary debugger console functionality through COM1. For details of Z-Tag and BUR operation, see the ZFx86 Data Book provided on the MZ104+ Quickstart CD or available for download at www.ZFMicro.com.

BUR /BOOT ROM select (JP8)		
JP8	BUR Mode OFF	Boot ROM* ON

Table 7: BUR/BOOT ROM Select

* Factory Setting

3.6 CLOCK MULTIPLIER SELECT (JP9, JP10)

The clock multiplier selection jumper sets the system clock for the MZ104+ core. The CPU operating speed is determined by:

$$\text{CPU frequency ratio} * \text{System clock (33MHz or 64MHz)}$$

For example, using 2X ratio with the System clock at 33 MHz :
the CPU speed will be $(2 * 33) = 66 \text{ MHz}$

Jumper CPU Frequency ratio	JP9	JP10
1x *	ON	ON
2x	OFF	ON
3X	OFF	OFF

Table 8: Clock Multiplier Select

* Factory Setting

3.7 WATCHDOG SELECT (CN16)

CN16 allows the user to select the watchdog input line.

WATCHDOG select (CN16)	External	Internal	None
CN16	1-2	2-3	None*

Table 9: WATCHDOG Select

* Factory Setting

3.8 ZTAG LED/RESET SELECT (CN18)

CN18 allows the user to activate the LED of the Ztag dongle or use the line to drive the master reset of the CPU board.

ZTAG LED/RESET select (CN18)	RESET linked	LED active
CN18	1-2	2-3*

Table 10: ZTAG LED/RESET Select

* Factory Setting

CHAPTER 4 - CONNECTORS

Connectors on the MZ104+ are provided to interface external devices such as a hard disk drive, floppy drive, and keyboard.

MZ104+ Connector List	
Connector Label	Function
CN1	USB Connector
CN2	Z-tag connector for field flash update or user code execution
CN3	PC/104+ connector
CN4	External power connector
CN5	Parallel port connector
CN6	Floppy drive connector
CN7	Utility connector for keyboard, mouse, battery and speaker
CN8	COM1 serial port connector
CN9	COM2 serial port connector
CN10	Ethernet 2 10/100BaseT
CN11	Ethernet 1 10/100BaseT
CN12	IDE drive connector
CN13	PC104 connector (40-pin)
CN14	PC104 connector (64-pin)
CN15	SO-DIMM memory socket
CN16	Watchdog trigger source
IC23	DiskOnChip socket

Table 7: MZ104+ Connector List

Note: Pin-1 of each connector on the MZ104+ is designated by a small white dot on the PCB. Pin-1 on the connector should line up with pin-1 of the corresponding mating connector on the cable.

4.1 USB CONNECTOR (CN1)

The MZ104+ provides two USB (Universal Serial BUS) interfaces that give complete plug-and-play support for external devices.

USB Connector (CN1)			
Pin	Signal	Pin	Signal
1	USBVCC2	2	USBD2F-
3	USBD2F+	4	GND
5	USBVCC1	6	USBD1F-
7	USBD1F+	8	GND

Table 8: USB Connector

4.2 Z-TAG CONNECTOR (CN2)

The Z-Tag connector (CN2) is a 14-pin connector that interfaces with the Z-Tag Dongle allowing for easy field flash updates or user code execution. Please refer to the Z-Tag and BUR chapter of the ZFx86 Data Book for complete details. A *Z-Tag Manager* utility program and manual are provided on the MZ104+ Quickstart CD and are available for download at www.ZFMicro.com. The Z-Tag Dongle, part number ZFx86DONGLE-1, is available from Tri-M Systems.

4.3 PC/104+ CONNECTOR (CN3)

The MZ104+ incorporates all the features of a PC/104 board with the added advantage of the high speed PCI bus. The PCI Mechanical interface is a stackable 30x4 header. This interface carries all of the required PCI signals per *PCI Local Bus Specification Version 2.1*. Signals are assigned in the same relative order as in the PCI Local Bus Specification, but transformed to the corresponding header connector pins.

PC/104+ Bus Connector (CN3)				
Pin	A	B	C	D
1	GND	NC	+5V	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	PMEX
7	AD14	AD13	GND	AD12
8	+3.3V	CBE1	AD15	+3.3V
9	SERR	GND	SB0	PAR
10	GND	PERR	+3.3V	SDONE
11	STOP	+3.3V	LOCK	GND
12	+3.3V	TRDY	GND	DEVSEL
13	FRAME	GND	IRDY	+3.3V
14	GND	AD16	+3.3V	C/BE2
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	N/A	GND	N/A	IDSEL2
19	AD24	C/BE3	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	N/A	GND	N/A	VI/O
24	GND	REQ2	+5V	N/A
25	N/A	VI/O	GNT2	GND
26	+5V	N/A	GND	N/A
27	CLK PCI 2	+5V	CLK PCI 3	GND
28	GND	INTD	+5V	RST
29	+12V	N/A	N/A	INTB
30	-12V	NC	NC	GND

Table 9: 32-bit PC/104+ Bus

Caution!
The MZ104+ supports 3.3V PC/104+ modules only.
If a 5V module is installed, it will damage the MZ104+.

Note: If stacking an expansion PC/104+ module on the topside of the MZ104+, please remove PC/104+ pin protective shroud on the expansion module.

4.4 EXTERNAL POWER (CN4)

The MZ104+ can be powered by supplying 5VDC and ground to CN4. Alternatively, the MZ104+ can be powered by supplying 5VDC through the 16-bit PC104 connector (CN13) with a PC104 power supply such as the Tri-M Engineering [HE104](#) or [HESC-104](#).

External Power (CN4)	
Pin Number	Signal
1	Vcc +5V
2	GND

Table 10: External Power Connector

4.5 PARALLEL INTERFACE (CN5)

The MZ104+ parallel port is fully compatible with the PC/AT parallel port. In the extended mode, it functions as a PS/2-like bi-directional port. In Extended Capabilities Port (ECP) mode, it is IEEE 1284 compliant, including level 2.

The parallel ports uses the following PC resources when enabled:

Parallel Port	Typical Usage	I/O Address	Standard Interrupt
Parallel 1	LPT1	378H – 37 Fh	IRQ7

Table 11: Parallel Port Resources

The default interrupt for parallel port LPT1 is IRQ7. The parallel port output signals provide up to 14-mA drive current. RC filters are provided for noise suppression. The parallel port signals appear on CN5, a dual-row ribbon-cable pin edge connector. The port may be cabled to appear on a standard PC DB-25 connector. A DB-25 connector and cable are provided for this purpose in the optional MZ104+ cable kit. The following table shows the parallel port signals appearing on CN5 and the equivalent pin out on a DB-25 connector.

CN5	DB-25 Pin	Signal	Function	In/Out	CN5	DB-25 Pin	Signal	Function	In/Out
1	1	STRB-	Output data strobe	OUT	2	14	AUTOFD-	Auto feed	OUT
3	2	PD0	Data bit 0	I/O	4	15	ERR-	Printer error	IN
5	3	PD1	Data bit 1	I/O	6	16	INIT-	Initialize printer	OUT
7	4	PD2	Data bit 2	I/O	8	17	SLCTIN-	Selects printer	OUT
9	5	PD3	Data bit 3	I/O	10	18	GND	Signal Ground	N/A
11	6	PD4	Data bit 4	I/O	12	19	GND	Signal Ground	N/A
13	7	PD5	Data bit 5	I/O	14	20	GND	Signal Ground	N/A
15	8	PD6	Data bit 6	I/O	16	21	GND	Signal Ground	N/A
17	9	PD7	Data bit 7	I/O	18	22	GND	Signal Ground	N/A
19	10	ACK-	Character acknowledged	IN	20	23	GND	Signal Ground	N/A
21	11	BUSY	Printer busy	IN	22	24	GND	Signal Ground	N/A
23	12	PE	Out of paper	IN	24	25	GND	Signal Ground	N/A
25	13	SLCT	Printer selected	IN	26	N/A	GND	Signal Ground	N/A

Table 12: Parallel Port Connections

Note: CN5 is an edge mounted PCB connector with odd number pins located on the “top”, and even number pins on the “bottom”.

4.6 FLOPPY INTERFACE (CN6)

The floppy interface provides the signal to control one 3 ½ " or 5 ¼" floppy drive. The default interrupt request for the floppy interface is IRQ6.

Floppy Connector (CN6)					
Pin	Signal	Function	Pin	Signal	Function
1	VCC5V	+5V	2	INDX	Index
3	VCC5V	+5V	4	DRX0	Drive select 0
5	VCC5V	+5V	6	DSKCHGX	Disk Change
7	NC	-	8	NC	-
9	NC	-	10	MTRXO	Motor On
11	NC	-	12	DIRX	Direction Select
13	NC	-	14	STEPX	Step
15	GND	Ground	16	WDATAX	Write data
17	GND	Ground	18	WGATEX	Write gate
19	GND	Ground	20	TRKX0	Track 00
21	GND	Ground	22	WPX	Write Protect
23	GND	Ground	24	RDATAX	Read data
25	GND	Ground	26	HDSELX	Side one select

Table 13: Floppy Interface

4.7 UTILITY PORT (CN7)

The utility connector provides the following inputs and outputs:

- Keyboard
- PS/2 mouse
- Infrared port
- Speaker
- CMOS backup battery
- Watchdog trigger source
- Hardware reset
- Hard drive LED

Signals on CN7 can be terminated using the MZ104+ utility board. This board provides the appropriate connectors for all the signals.

Utility Connector (CN7)		
Pin	Signal	Function
1	HDDLEDOUT	Hard drive LED output (8mA source)
2	RESETX	Hardware reset
3	IRRXD	Infrared receive
4	IRTXD	Infrared Transmit
5	WD_EXT	External Trigger Source for watchdog timer
6	VBAT_CLK	RTC backup battery +V terminal (3.6V)
7	SDA	SMBus data
8	KBMPWR	+5V
9	GND	Ground
10	SCL	SMBus clock
11	SPKOUT	Speaker output
12	KBLOCKX	Keyboard lock
13	MCLKX	P/S2 mouse clock
14	MDATX	P/S2 mouse data
15	KBCLKX	Keyboard clock
16	KBDATX	Keyboard data

Table 14: Utility connector

4.8 SERIAL INTERFACES (CN8, CN9)

The MZ104+ provides two PC-compatible asynchronous serial ports. Typically, DOS and Windows treat the serial ports as COM1 and COM2 devices. Standard system resources are allocated to the serial ports:

Serial Port	Typical Usage	I/O Address	Standard Interrupt
Serial 1 (CN8)	COM1	3F8h–3FFh	IRQ4
Serial 2 (CN9)	COM2	2F8h–2FFh	IRQ3

Table 15: Serial Port Resources

Serial 1 and Serial 2 port can be disabled using BIOS SETUP. When disabled, the port's I/O address is made available for other expansion devices on the 16-bit BUS.

COM1 (CN8) Details

Serial port COM1 and COM2 supply a full complement of input and output handshaking lines. These signals are at standard RS232C levels. The RS232C level converters provide the required RS232C voltage levels with internal +5 volt to ± 9 volt converters.

DB-9 Pin	CN8	Signal	Function	In/Out	DB-9 Pin	CN8	Signal	Function	In/Out
1	1	DCD1	Serial 1 Data Carrier Detect	INPUT	6	2	DSR1	Serial 1 Data Set Ready	INPUT
2	3	RXD1	Serial 1 Receive Data	INPUT	7	4	RTS1	Serial 1 Request To Send	OUTPUT
3	5	TXD1	Serial 1 Transmit Data	OUTPUT	8	6	CTS1	Serial 1 Clear To Send	INPUT
4	7	DTR1	Serial 1 Data Terminal Ready	OUTPUT	9	8	RI1	Serial 1 Ring Indicator	INPUT
5	9	GND	Signal Ground			10	N/C	No connection	

Table 16: Serial Port COM1 Connection

COM2 (CN9) Details

DB-9 Pin	CN9	Signal	Function	In/Out	DB-9 Pin	CN9	Signal	Function	In/Out
1	1	DCD1	Serial 1 Data Carrier Detect	INPUT	6	2	DSR1	Serial 1 Data Set Ready	INPUT
2	3	RXD1	Serial 1 Receive Data	INPUT	7	4	RTS1	Serial 1 Request To Send	OUTPUT
3	5	TXD1	Serial 1 Transmit Data	OUTPUT	8	6	CTS1	Serial 1 Clear To Send	INPUT
4	7	DTR1	Serial 1 Data Terminal Ready	OUTPUT	9	8	RI1	Serial 1 Ring Indicator	INPUT
5	9	GND	Signal Ground			10	N/C	No connection	

Table 17: Serial Port COM2 Connection

Note: CN8 and CN9 are an edge mounted PCB connector with odd number pins located on the "top", and even number pins on the "bottom". Pin-1 is designated by a white dot on the PCB.

4.9 ETHERNET 10/100 BaseT (CN10, CN11)

The MZ104+ is equipped with two Intel 82559ER fast Ethernet controllers supporting 10Mb/s and 100 Mb/s N-way auto-negotiating operation.

Ethernet2 (CN10)				Ethernet1 (CN11)			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	TX2+	2	TX2-	1	TX1+	2	TX1-
3	RX2+	4	NC	3	RX1+	4	NC
5	NC	6	RX2-	5	NC	6	RX1-
7	NC	8	NC	7	NC	8	NC

Table 18: Ethernet Connections

4.10 IDE INTERFACE (CN12)

The MZ104+ has a PCI bus mastering ATA-4 compatible IDE controller. The IDE controller supports Ultra DMA, Multi-word DMA, and all Programmed I/O (PIO) modes. Up to two drives can be connected, in a master-slave arrangement. Generally, the first hard disk drive (master) will appear as the C drive to DOS. The second drive, if attached, will appear as D.

Resource	Function
I/O Address (1F0h-1F7h)	Hard Disk Interface
IRQ14	Interrupt

Table 19: Hard Disk Resources

Use SETUP to auto-detect your attached hard drives. For further details about setting up IDE hard disk parameters See the SETUP description in the BIOS manual provided on the MZ104 Quickstart CD or available for download at www.ZFMicro.com.

IDE Interface (CN12)							
Pin	Signal Name	Function	In/Out	Pin	Signal Name	Function	In/Out
1	RESET	Reset signal from host	OUT	2	GND	Ground	
3	DD7	Data bit 7	I/O	4	DD8	Data bit 8	I/O
5	DD6	Data bit 6	I/O	6	DD9	Data bit 9	I/O
7	DD5	Data bit 5	I/O	8	DD10	Data bit 10	I/O
9	DD4	Data bit 4	I/O	10	DD11	Data bit 11	I/O
11	DD3	Data bit 3	I/O	12	DD12	Data bit 12	I/O
13	DD2	Data bit 2	I/O	14	DD13	Data bit 13	I/O
15	DD1	Data bit 1	I/O	16	DD14	Data bit 14	I/O
17	DD0	Data bit 0	I/O	18	DD15	Data bit 15	I/O
19	GND	Ground		20	KEY	Keyed pin	N/C
21	DREQ	DMA 0 Request	OUT	22	GND	Ground	
23	D1OW	Write strobe	OUT	24	GND	Ground	
25	D1OR	Read strobe	OUT	26	GND	Ground	
27	IORDY	I/O channel ready	IN	28	GND	Ground	OUT
29	IDEPDACK	DMA 0 Acknowledge	IN	30	GND	Ground	
31	IRQ14	Drive interrupt request	IN	32	IOCS16	I/O Chip Select 16	In
33	DA1	IDE Address 1	Out	34	RSVD	Reserved	N/C
35	DA0	IDE Address 1	Out	36	DA2	IDE Address 2	Out
37	HDCS0	IDE Chip Select 0	Out	38	HDCS1	IDE Chip Select 1	Out
39	HDDLED			40	GND	Ground	
41	VCC5V	+5V		42	VCC5V	+5V	
43	GND	Ground		44	NC	-	

Table 20: IDE Drive Interface

NOTE: For maximum reliability, IDE drive cables should be limited to 18 inches or less in length.

4.11 PC/104 CONNECTOR (CN14 AND CN13)

CN13 and CN14 provide the flexibility to attach PC/104 expansion modules to the MZ104+. These modules perform the functions of traditional add-in cards in a PC environment. All data, address and control signals are able to sink 10mA and source 8mA.

8-bit 64-pin Connector (CN14)

PC/104 8-bit Connector (CN14)			
Pin #	Signal	Pin #	Signal
A1	IOCHK	B1	GND
A2	SD7	B2	RSTDRV
A3	SD6	B3	+5V
A4	SD5	B4	IRQ9
A5	SD4	B5	N/A
A6	SD3	B6	N/A
A7	SD2	B7	-12V
A8	SD1	B8	ZEROWS
A9	SD0	B9	+12V
A10	IOCHRDY	B10	KEY
A11	AEN	B11	SMEMW
A12	SA19	B12	SMEMR
A13	SA18	B13	IOW
A14	SA17	B14	IOR
A15	SA16	B15	N/A
A16	SA15	B16	N/A
A17	SA14	B17	DACK1
A18	SA13	B18	DRQ1
A19	SA12	B19	REFRESH
A20	SA11	B20	CLK8MHZ
A21	SA10	B21	IRQ7
A22	SA9	B22	N/A
A23	SA8	B23	IRQ5
A24	SA7	B24	IRQ4
A25	SA6	B25	IRQ3
A26	SA5	B26	N/A
A27	SA4	B27	TC
A28	SA3	B28	BALE
A29	SA2	B29	+5V
A30	SA1	B30	CLK14MHZ
A31	SA0	B31	GND
A32	GND	B32	GND

Table 21: PC/104 8-bit Interface

16-bit 40-pin Connector (CN13)

PC/104 16-bit Connector (CN13)			
Pin #	Signal	Pin #	Signal
C0	GND	D0	GND
C1	SBHEX	D1	MCS16
C2	SA23	D2	IOCS16
C3	SA22	D3	IRQ10
C4	SA21	D4	IRQ11
C5	SA20	D5	IRQ12
C6	SA19	D6	IRQ15
C7	SA18	D7	N/A
C8	SA17	D8	N/A
C9	MEMR	D9	N/A
C10	MEMW	D10	DACK5
C11	SD8	D11	DRQ5
C12	SD9	D12	N/A
C13	SD10	D13	N/A
C14	SD11	D14	N/A
C15	SD12	D15	N/A
C16	SD13	D16	+5V
C17	SD14	D17	MASTER
C18	SD15	D18	GND
C19	KEY	D19	GND

Table 22: PC/104 16bit Interface

4.12 SO-DIMM SOCKET (CN15)

The SO-DIMM memory socket accommodates one industrial standard 144-pin SO-DIMM memory module. The memory type compatible with the MZ104+ is 32-bit, 3.3V PC100 or PC66 SDRAM. The MZ104+ can handle a maximum of 128MB of SDRAM³. The BIOS automatically senses the amount of memory installed in your system and saves that information in the CMOS SETUP memory when you save the SETUP information. For further information on MZ104+ Memory, please refer to [Appendix 1](#) of this manual.

Note: The ZFx86 processor on the MZ104+ is a 32-bit processor thereby requiring 32-bit SO-DIMM memory modules.

MZ104+ SDRAM SO-DIMM modules (8 - 64MB) are available from [Tri-M Systems](#).

Part number: MEM-XXMB-MZ (XX = capacity in MB)

Example: MEM-32MB-MZ is a 32MB module

³ Maximum available in a standard size SO-DIMM module is 64MB. For 128MB, an oversized card must be used. This is currently not available from Tri-M Engineering.

4.13 WATCHDOG TIMER (CN16)

The ZFx86 chip on the MZ104+ offers two watchdog timers, WD1 (16-bit counter) and WD2 (8-bit counter). Both timers are programmable. The maximum period for WD1 is two seconds while the maximum period for WD2 is 7.2ms. WD2 starts counting down after WD1 expires. When WD2 counter reaches zero, it will unconditionally cause system reset.

The watchdog timer will alarm if not triggered by the system or application at least once every 2 seconds. If the watchdog timer does not receive its reset (“tickle”) after 2 seconds has elapsed, it generates its alarm signal. The watchdog timer alarm is reset (“tickled”) by toggling the WDI signal or writing to index 0x10h of the ZF-Logic I/O space. The watchdog is triggered continuously (disabled) if jumper is installed at 2-3 of CN16. This arrangement allows watchdog input (WDI) be toggled by watchdog alarm output (WDO) in a self-triggering fashion. If jumper is installed at 1-2 of CN16, the watchdog will be triggered by an external signal from pin12 of CN7. You must provide this trigger signal.

Jumper Position	Function
1-2	External source to reset watchdog
2-3	Disable watchdog

Table 23: Watchdog Jumper

The watchdog timer alarm signal (WDO) can be programmed to generate the following response when corresponding bit is set at the watchdog control register in the ZF-Logic I/O space.

- Non-maskable interrupt (NMI)
- System controller interrupt (SCI)
- System Management interrupt (SMI)
- Hardware reset

For further information on the Watchdog Timer and for programming detail, please consult the ZFx86 data book provided on the MZ104+ Quickstart CD and available for download at www.zfmicro.com.

Note: The watchdog timer is not enabled at power up by the BIOS. Therefore, when the jumper is installed at CN16 it does not affect the operation of the MZ104+.

4.14 DiskOnChip SOCKET (IC23)

The MZ104+ provides a 32-pin DIP socket, which can be populated with either an M-Systems' DiskOnChip 2000 and DiskOnChip Millennium product. Before the DiskOnChip can be accessed, the memory windows, which the socket is mapped to, must be enabled. This is accomplished by the ISA memory parameters in the CMOS setup. Please consult the **ZFx86 BIOS Supplement** manual for detailed explanation on setting up memory windows. To enable the socket, please follow the steps below:

1. Enter CMOS setup by pressing function key **F2** prior to booting OS from boot media.
2. From the menu bar of the **Main** setup screen, choose **Advanced**.
3. From the **Advanced Setup Screen**, choose **Advanced Chipset Control**.
4. Set **Onboard RFD** to **Disabled**.
5. From **Advanced Chipset Control**, choose **ISA Memory chip select setup**
6. Set **Memory Window_Mem_CS3** as follows:
 - Window Size: 1
 - Window Base: D0
 - Window Page: F30
 - Window Data Width: 8-Bit
7. Save setup & exit
8. Reboot computer

Note: The memory window setting is lost when the MZ104+ is powered down unless a backup battery is provided. Use ZF Micro Devices' ZEB utility to set defaults into the BIOS. ZEB utility is provided in the BIOS folder on the MZ104+ quickstart CD and is also available for download at www.zfmicro.com

Pin Name	Description	Pin Number	Direction
A0 – A12	Address bus	4-12, 23, 25-27	Inputs
D0 – D7	Data bus	13-15, 17-21	I/O
CE/	Chip Enable	22	Input
OE/	Output Enable	24	Input
WE/	Write Enable	31	Input
NC	Not Connected	1, 2, 3, 28, 29, 30	
VCC	Power	32	
GND	Ground	16	

Table 24: DiskOnChip Socket (IC23)

CHAPTER 5 – SETUP

5.1 MZ104+ INTERRUPT AND I/O PORT ASSIGNMENTS

IRQ Number	MZ104 Assignment
0	Systems timer (not available for other devices)
1	Keyboard controller (not available for other devices)
2	Second PIC cascade (not available for other devices)
3	Serial port two (COM2:)
4	Serial port one (COM1:)
5	Unassigned
6	Floppy Disk controller
7	Parallel (printer) port one (LPT1:)
8	Real-time clock (RTC)
9	INTA
10	INTB
11	USB / INTC
12	PS/2 Mouse /INTD
13	Math coprocessor
14	Primary IDE
15	Secondary IDE

Note: INTA through INTD are PCI interrupt request lines. Ethernet controllers are automatically assigned to free IRQs

Table 25: MZ104+ Interrupt Assignments

I/O Address	Hardware
0000 - 000F	DMA Controller
0020 - 0021	PIC
0022 - 0021	Motherboard Resources
0040 - 0043	System Timer
0060 - 0060	Keyboard
0061 - 0061	Systems Speaker
0064 - 0064	Keyboard
0070 - 0071	System CMOS / Real time clock
0081 - 008F	DMA Controller
0092 - 0092	Motherboard Resources
00A0 - 00A1	PIC
00C0 - 00DF	DMA Controller
00F0 - 00FF	Numeric Data Processor
02F8 - 02FF	Communications Port B
0378 - 037F	Printer Port
03F0 - 03F5	Floppy Disk Controller
03F7 - 03F7	Floppy Disk Controller
03F8 - 03FF	Communications Port A
0480 - 048F	Motherboard Resources
04D0 - 04D1	Motherboard Resources
0778 - 077F	Printer Port
0CF8 - 0CFE	PCI Bus
AC00 - AC1F	Motherboard Resources
AC80 - AC9F	Motherboard Resources

Table 26: MZ104+ I/O Port Assignments

5.2 BIOS SETUP

The MZ104+ system BIOS (Basic Input Output System) supports a standard SETUP function to configure system parameters. The BIOS uses these parameters to establish default conditions during system initialization, both during the Power On Self Test (POST) phase, and during system boot.

Using SETUP

To enter the SETUP function, press the <F2> key during POST.

Note: When you change SETUP parameters, the new values do not take effect until the system is rebooted.

For details about how to set the various parameters using SETUP, please refer to the ZFx86 BIOS Users Manual Supplement and the PhoenixBIOS 4.0 Rev 6 manual provided on the MZ104+ Quickstart CD or available for download at www.ZFMicro.com.

APPENDIX 1 – MZ104+ MEMORY INFORMATION

The ZFx86 processor on the MZ104+, like other X'86 processors, requires “main memory”. The main memory of the ZFx86 must be SDRAM (Synchronous Dynamic Random Access Memory). The SDRAM controller of the ZFx86 can access SDRAM chips with densities from 16Mbit to 128Mbit.

Tri-M Engineering uses a modular memory approach with the MZ104+, thus allowing customers to select the size of memory that best fits their application. Standard DIMM modules are not used as they are physically too large to fit the PC/104 footprint of the MZ104+. Similarly, 72-pin SO-DIMMS are not used as the connectors are increasingly difficult to source primarily because laptop computers have moved to the 144-pin SO-DIMMS. The problem that arises with the common laptop 144-pin SO-DIMMS is that they are designed for 64-bit processors whereas the ZFx86 can handle a maximum of 32-bit. This means that either only half the memory can be utilized, or “custom” memory cards are required. Some of the standard memory cards on the market can be “depopulated”, thus not requiring the manufacturer to produce a custom PCB. However, not all SO-DIMM memory cards can be depopulated and still work with the ZFx86. When SDRAM chips of 16-bit width are used, some manufacturers wire the one half of the memory into the second 32-bit. This makes for an efficient PCB layout, but when a chip is depopulated, it also depopulates the lower 32 bits. The lower 32-bits are the ones the ZFx86 processor requires.

Note: For those who wish to manufacture their own SDRAM SO-DIMM memory modules, Tri-M Engineering will supply the schematics and Gerber files upon request free of charge.

APPENDIX 2 - LITERATURE REFERENCES

The following references are for information about the PC/104 and PC/104+ architecture, the PC DOS, and the PC BIOS.

ISA System Architecture

MindShare, Inc., Tom Shanley and Don Anderson
Internet: mindshar@interserv.com
CompuServe: 72507,1054
Published by Addison Wesley, Inc.

AT Bus Design

Edward Solari
Anabooks
12145 Alta Carmel Ct., Suite 250
San Diego, CA 92128
ISBN 0-929392-08-6

Personal Computer Bus Standard P996

Institute of Electrical and Electronic Engineers, Inc.
445 Hoes Lane
Piscataway, NJ 08854

PC Interrupts

PC Interrupts, Ralf Brown,
Addison/Wesley.

BIOS Reference

System BIOS for IBM PC/XT/AT Computers, Phoenix, Addison/Wesley

PC/104 Consortium

809 B-175 Cuesta Drive,
Mountain View, CA 94040
Phone: 415 903-8304
FAX: 415 967-0995

DiskOnChip

M-Systems Corp
8371 Central Avenue Suite A
Newark, CA 94560
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FAX: 510-494-5545

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ZF Micro Devices, Inc.
1052 Elwell Court
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