

Versatile Computer Module with ARM-920T core

The VCMA9 is a highly integrated industrial single board computer in a small form factor. It is built around the S3C2410 microprocessor from Samsung that uses the ARM920T core and additionally implements a complete set of common system peripherals. Besides the features of the S3C2410, the VCMA9 offers Ethernet, CAN and DAC. As main memory up to 128MB SDRAM are available onboard and as mass storage device a NAND-Flash is soldered.

Via expansion bus connector the system can be further more adapted to your needs. Integration of the VCMA9 into a system is facilitated by the fact that all connectors have 2mm pitch. The VCMA9 can be used in a standard operating environment without the necessity of a fan.

All these features make the module extremely flexible and versatile. It is well suited for applications where a none x86 architecture is preferred and that do requiring small-size, high-performance and low-power.

Features

- S3C2410 Processor with ARM920T core
- Processor clock up to 200 MHz
- Up to 128MByte SDRAM onboard
- Up to 128Mbyte NAND-Flash onboard
- 10 Mbit/s Ethernet Controller
- CAN 2.0B Stand-alone Controller
- LCD Controller (STN and TFT support)
- Two USB Ports
- Three RS232 ports
- 8-channel ADC
- 4-channel DAC
- Up to 64 digital I/O's
- 32-bit expansion bus
- Low power consumption



VCMA9-1 fully equipped

TABLE OF CONTENTS

1. INTRODUCTION	4
1.1 About this manual	4
1.2 Safety precautions and handling	4
1.3 Electrostatic discharge (ESD) protection	4
1.4 Equipment safety	4
2. GENERAL INFORMATION AND SPECIFICATIONS.....	5
2.1 Product Description	5
2.2 Specifications	5
2.2.1 Electrical	5
2.2.2 Physical / Power.....	8
2.2.3 Environment.....	8
2.3 Dimensions.....	9
3. PREPARATION FOR USE.....	10
3.1 Parts location.....	10
3.2 Switch settings.....	11
3.2.1 DIP switch S1 – DAC High and Low Reference Input Switch	11
3.2.2 DIP switch S2 – ADC Reference Voltage and LCD Voltage Switch	11
3.2.3 DIP switch S3 – Hardware Configuration Switch	11
3.3 Indicators.....	12
3.4 Connectors	12
3.4.1 J1 - USB connector	12
3.4.2 J2 – Serial 0 Header connector	13
3.4.3 J3 – Serial1/2 Header connector	13
3.4.4 J4 – 10Base-T Header connector	14
3.4.5 J5 – CAN Header connector.....	14
3.4.6 J6 – Special Ethernet connector.....	14
3.4.7 J7 – Special Clock connector	15
3.4.8 J8 – Debug / JTAG connector	15
3.4.9 J9 – Special SEC TFT connector.....	15
3.4.10 J10 – Power, I2C & SPI connector.....	16
3.4.11 J11 – Digital IO connector	18
3.4.12 J12 – Analog IO connector	18
3.4.13 J13 – I2S, SD & Timer connector	18
3.4.14 J14 – LCD & Touch connector.....	19
3.4.15 J15 – Expansion Bus connector	20
4. OPERATION	21
4.1 Block diagram.....	21
4.2 Memory Controller	22
4.3 NAND-Flash Controller	23
4.4 Interrupt Controller.....	24
4.4.1 Interrupt Mode.....	24
4.4.2 Interrupt Pending Register.....	24
4.4.3 Interrupt Mask Register	24
4.4.4 Interrupt Sources.....	25
4.4.5 Mapping of external IRQ pins	26
4.5 DMA Controller	27
4.5.1 DMA Request Sources	27
4.5.2 DMA Operation	27
4.6 Digital Analog Converter (DAC)	29

4.6.1	DAC Registers	29
4.6.2	Communication via SPI-0	30
4.7	Connecting a LCD	31
4.8	Connecting a touch.....	31
4.9	Extension registers	32
4.9.1	PLD Register.....	32
4.9.2	NIC Register	32
4.9.3	CAN Register	32
4.9.4	MISC Register.....	33
4.9.5	GPCD Register	33
4.9.6	BOARD Register	34
4.9.7	SDRAM Register.....	34
5.	SUPPORT INFORMATION	35
5.1	MPL AG.....	35
5.2	Related documents.....	35
5.3	Production serial and revision number	35
5.4	VCMA9-Baseboard from MPL.....	35
6.	APPENDIX.....	36
6.1	Mounting VCMA9 as add-on board	36
6.2	Power up the VCMA9	36

1. Introduction

1.1 About this manual

This manual assists the installation and initialization procedure by providing all hardware related information necessary to handle and configure the VCMA9.

For all bootloader related information please refer to the 'U-Boot for the VCMA9' User Manual (MEH-10082-002) supplied by MPL AG or your local VCMA9 supplier. The 'U-Boot for VCMA9' User Manual should also be available on the internet under "<http://www.mpl.ch>" in PDF format.

This manual is written for technical personnel responsible for integrating the VCMA9 into their system.

1.2 Safety precautions and handling

For personal safety and safe operation of the VCMA9, follow all safety procedures described here and in other sections of the manual.

- Power must be removed from the system before installing (or removing) the VCMA9 to prevent the possibility of personal injury (electrical shock) and/or damage to the product.
- Handle the product carefully, i.e., dropping or mishandling the VCMA9 can cause damage to assemblies and components.
- Do not expose the equipment to moisture.

WARNING

There are no user-serviceable components on the VCMA9

1.3 Electrostatic discharge (ESD) protection

Various electrical components within the product are sensitive to static and electrostatic discharge (ESD). Even a non-sensible static discharge can be sufficient to destroy or degrade a component's operation!

Following the precautions listed below will avoid ESD-related problems:

- Use a properly installed anti static pad on your work surface.
- Wear wrist straps and observe proper ESD grounding techniques.
- Leave the unit in its anti static cover until you are prepared to install it in the desired environment. When it is out of its protection cover, place the unit on the properly grounded anti static work surface pad.
- Do not touch any components on the product. Handle the product by its card edges.

1.4 Equipment safety

Great care is taken by MPL that all its products are thoroughly and rigorously tested before leaving the factory to ensure that they are fully operational and conform to specification. However, no matter how reliable a product, there is always the remote possibility that a defect may occur. The occurrence of a defect on this device may, under certain conditions, cause a defect to occur in adjoining and/or connected equipment. It is the user's responsibility to ensure that adequate protection for such equipment is incorporated when installing this device. MPL accepts no responsibility whatsoever for such kind of defects, however caused.

2. General information and specifications

This chapter provides a general overview over the VCMA9 and its features. It outlines the electrical and physical specifications of the product and its power requirements.

2.1 Product Description

The VCMA9 is a high-performance, low-power and compact single board computer. As core component Samsung's S3C2410 Microprocessor is equipped. This processor is controlled through a 16/32-bit ARM920T CPU core with implemented Memory Management Unit and separate 16kB instruction and data cache. Also integrated on the die are many intelligent peripheral sub-modules that dramatically increase functionality. Besides the features of the S3C2410, the VCMA9 is loaded with Ethernet, CAN and DAC. As main memory up to 128MB SDRAM are available on board and as mass storage device a NAND-Flash is soldered. All these features make the board extremely flexible and versatile.

The signals of all on board peripherals, are combined on different 2mm pitch headers and sockets. So with some simple adapter boards the VCMA9 can be used as Stand-alone board. Also users are free to realize their own adapter-board and use the VCMA9 as add-on CPU-board. Via expansion bus connector it is possible to expand your system further more (e.g. with additional peripherals, memory and/or I/O's) to your needs.

Software development is simplified by the fact that the S3C2410 has an JTAG/MultiICE debug port implemented. The VCMA9 provides a 12pin header that interconnects this on-chip ARM debugger with a number of PC-based development tools (e.g. from Abatron). Because the VCMA9 does not base on the x86 architecture Operating Systems like Linux, WinCE, EPOC 32 or a RTOS are used. We provide you with the open source bootloader "ARMboot for VCMA9". Its main purpose is to initialize the hardware, setup the SDRAM and boot a kernel image. The ARMboot is closely related to Linux and special provision has been made to support booting of Linux kernel images.

2.2 Specifications

2.2.1 Electrical

Processor:

- Samsung S3C2410 16/32-bit RISC Microprocessor
- Includes ARM920T CPU core with MMU, 16kB instruction and 16kB data cache
- Integrated set of common peripherals
- Clock frequency up to 200 MHz
- Very low power consumption

Bootloader ROM:

- Up to 1MB Flash EEPROM (normal 512kB equipped)
- normally delivered with open source ARM-bootloader
- Easy bootloader update

Memory:

- Up to 128MByte SDRAM onboard

Storage:

- Up to 128MByte NAND-Flash onboard

Real Time Clock:

- Built in S3C2410 processor
- Full clock feature with alarm and time tick interrupt
- Can be backed with external battery

LCD controller:

- Built in S3C2410 processor
- Supported STN types: 4-bit single scan, 4-bit dual scan, 8-bit single scan
- up to 4k color STN LCD
- Supported TFT types: up to 8bpp palette color, 16bpp non-palette true-color and 24bpp color TFT
- Supports multiple screen size (640x480, 320x240, 160x160 and others)
- Maximum virtual screen size is 4Mbyte
- Selectable 3.3V or 5V panel signaling

Timers:

- Built in S3C2410 processor
- One 16-bit internal timer with DMA- or Interrupt-based operation
- Four 16-bit Timer with PWM
- Programmable duty cycle, frequency and polarity

Serial ports:

- Built in S3C2410 processor
- Three serial ports with RS232 signaling
- Standard transfer rates up to 115.2 kBaud
- ESD protected
- Selectable: - One port with handshake and two only Rx/Tx
- Two ports with handshake
- One full modem port (assembly option – demand by order)

A/D Converter:

- Built in S3C2410 processor
- 8 channel multiplexed, 10-bit resolution, max. 500ksp/s
- 2 channels can be used for touch screen interface

D/A Converter:

- Connected to SPI channel 0 of S3C2410
- Nonvolatile, 4 channel, 8-bit resolution DAC's
- With High and Low Reference Input

Digital I/O:

- Built in S3C2410 processor
- At least 8 (up to 64 possible)
- TTL level (3.3V interfaces with 5V tolerant input buffers)

Watchdog:

- Built in S3C2410 processor
- 16-bit watchdog Timer
- Interrupt request or system reset at time-out

I2C-Bus:

- Built in S3C2410 processor
- Serial, 8-bit bi-directional data transfer up to 400kbit/s
- 256kbit EEPROM connected to I2C-bus on board (selectable address via DIP switches)

SPI-Interface:

- Built in S3C2410 processor
- Two channels (Serial Peripheral Interface Protocol version 2.11)
- 2x8 bits Shift register for Tx/Rx, DMA- or Interrupt-based operation

I2S-Bus:

- Built in S3C2410 processor
- Serial, 8-/16-bit data transfer for audio interface with DMA-based operation
- Two 64 byte FIFO for Tx/Rx

SD Host Interface:

- Built in S3C2410 processor
- Compatible with SD Memory / IO Card Protocol version 1.0 and Multimedia Card Protocol version 2.11
- 64 bytes FIFO for Tx/Rx, DMA- or Interrupt-based operation

USB:

- Built in S3C2410 processor
- Two USB version 1.1 ports for serial transfers at 12 or 1.5 Mbit/s
- One fix Host port and one selectable as Host or Device port
- Complies with OHCI Rev. 1.0
- ESD protected

Ethernet:

- CS8900A Ethernet Controller
- IEEE802.3 10BASE-T port (10Mbit/s)
- Activity indicators for link status and network activity on board
- ESD protected

CAN:

- SJA1000 Stand-alone CAN Controller
- CAN 2.0B protocol compatibility (extended frame)
- Opto isolated interface with external supply 9V...18V_{DC}, 100mA max.
- ESD protected

Indicators:

- Power LED (green)
- Reset / Power Fail LED (red)

Expansion interface:

- 32 bit Databus
- 27 bit Addressbus and 3 free Chipselects
- Controlsignals including free IRQs, DMA, Clock and Reset

2.2.2 Physical / Power

Form factor:

Length: 90 mm (3.545 inches)
Width: 100 mm (3.945 inches)
Height: 8 mm (0.315 inch)

Weight:

Typical 65g (fully equipped)

Power supply:

Over 15-pin 2mm socket connector J10.

Input Power requirement:

+5V: +5V_{DC} ± 5%

Power consumption:

Typ. 300mA@5V (with Ethernet, CAN, 64MB SDRAM and 8MB NAND-Flash)

2.2.3 Environment

Temperature range:

0°C to +70°C @ 200 MHz CPU speed without heat sink
extended temperature range available

Relative humidity:

10% ... 90% non condensing

2.3 Dimensions

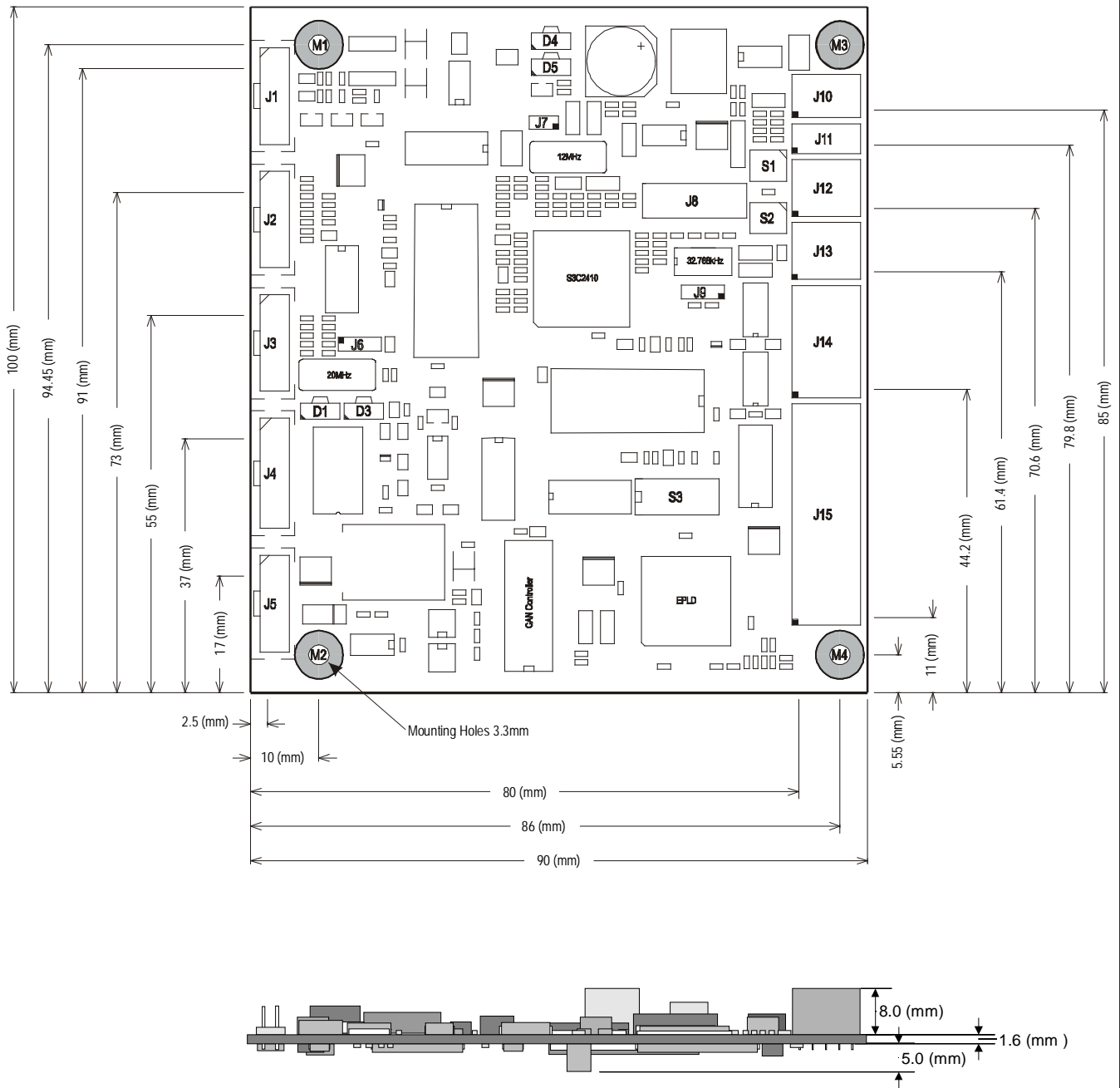


Figure 2.3.1 Dimensions VCMA9

3. Preparation for use

3.1 Parts location

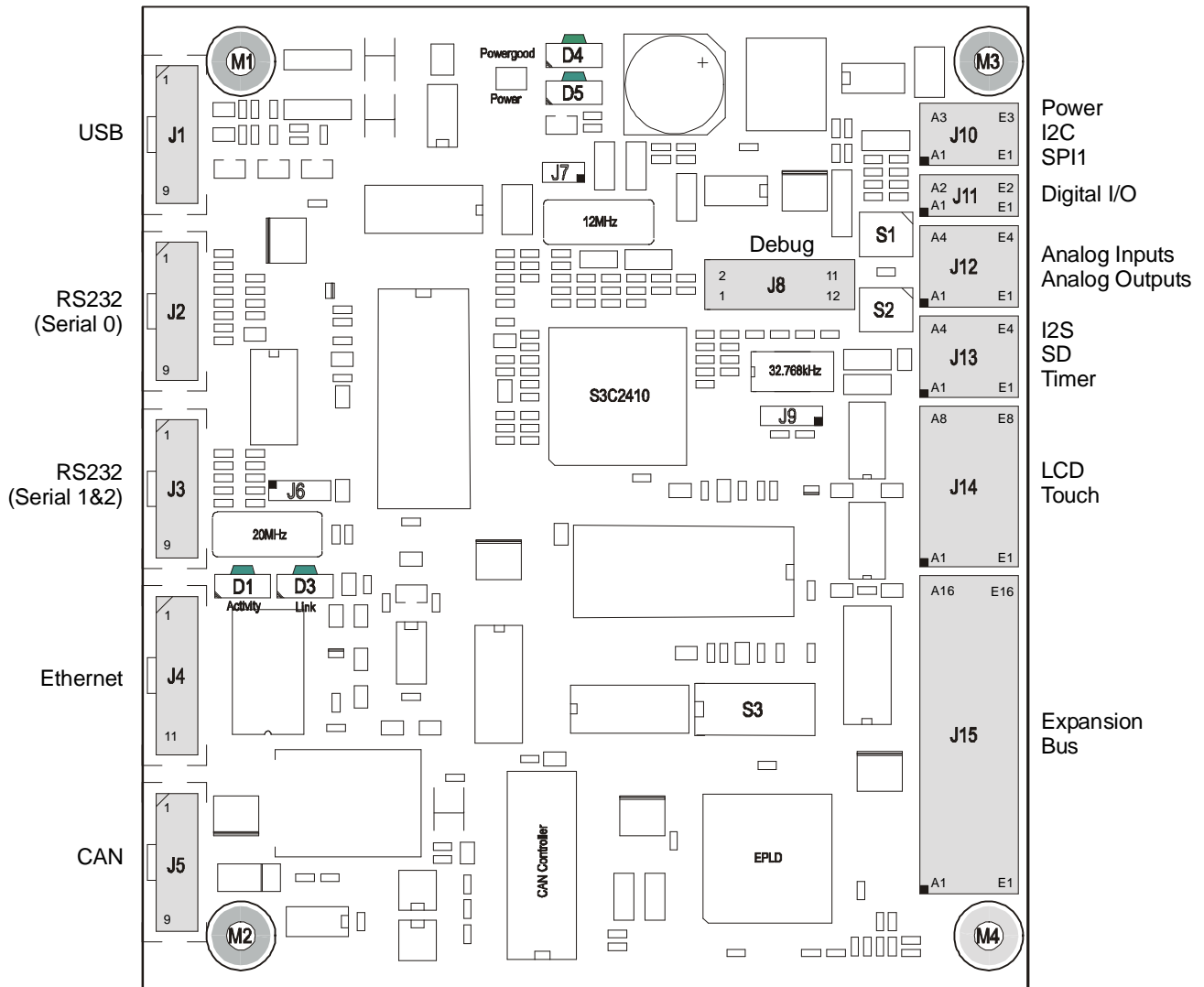


Figure 3.1.1 Parts location Top view

3.2 Switch settings

Default switch settings are bold.

3.2.1 DIP switch S1 – DAC High and Low Reference Input Switch

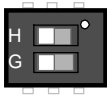
Switch	High-Position (left)	Low-Position (right)	S1
S1-1	DAC High Reference Voltage is +3.3V.	DAC High Reference Voltage is feed through Analog Input/Output socket (J12) pin D3 (AO_REFH).	
S1-2	DAC Low Reference Voltage is GND.	DAC Low Reference Voltage is feed through Analog Input/Output socket (J12) pin B3 (AO_REFL).	

Table 3.2.1 S1: DAC High and Low Reference Input Switch

Note:

- *DAC Reference Input Voltage Range for V_{REFH} and V_{REFL} must be between GND and +5V.*

3.2.2 DIP switch S2 – ADC Reference Voltage and LCD Voltage Switch

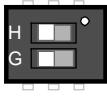
Switch	High-Position (left)	Low-Position (right)	S2
S2-1	ADC Reference Voltage is +3.3V.	ADC Reference Voltage is feed through Analog Input/Output socket (J12) pin A1 (AI_Vref).	
S2-2	LCD signal Voltage is +5V.	LCD signal Voltage is +3.3V.	

Table 3.2.2 S2: ADC Reference Voltage and LCD Voltage Switch

Note:

- *ADC Reference Voltage Range must be between GND and +3.3V.*

3.2.3 DIP switch S3 – Hardware Configuration Switch


Switch	On	Off	S3
S3-1	NAND-Flash spare area disabled	NAND-Flash spare area enabled	
S3-2	NAND-Flash write protected	NAND-Flash not protected	
S3-3	I2C EEPROM Address 0 = 0	I2C EEPROM Address 0 = 1	
S3-4	I2C EEPROM Address 1 = 0	I2C EEPROM Address 1 = 1	
S3-5	I2C EEPROM write protected	I2C EEPROM not protected	
S3-6	USB port1 is a Host port	USB port1 is a Device port	
S3-7	Boot from NAND-Flash	Boot from Boot-Chipselect Device (16-bit width)	
S3-8	Boot-Chipselect mapped to Expansion bus (J15) pin C15.	Boot-chipselect mapped to on board Bootloader-ROM	

Table 3.2.3 S2: Hardware Configuration Switch

DIP-switch default values are written in bold.

Caution: S3-1 always has to be OFF because the calculated ECC value of each page is stored in the NAND-Flash spare area! On VCMA9 with production revision C or higher this switch has no effect any more.

3.3 Indicators

There are four LED's on the board that are used as follows:

Ref	Color	Description	
D1	green	ACTIVITY	Lit when Network activity
D3	green	LINK	Lit when LAN Link is detected
D4	green	PWRGOOD	Lit when everything ok, dark if VCMA9 is in Reset
D5	yellow	POWER	Lit when internal power supplies are ok

Table 3.3.1 VCMA9 Indicators

3.4 Connectors

Signal names are according to the S3C2410 datasheet.

Connectors are shown as placed on VCMA9 board.
(Hold the board that way, that the CAN connector is in the under left corner)

3.4.1 J1 - USB connector

USB port 0 is always working as host port. USB port 1 can be used either as host port or as device port. The selection is made with switch3–6 (see 3.2.3).

Male header connector 2x5pin, 2mm pitch.

Type: Samtec TMM-105-02-L-D

Counterpart: Samtec Type SQT

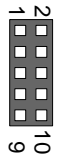
Number	Signal	Description	Pinout
1	VCC	Cable Power +5V _{DC} for Port0 (Host port)	
2	VCC / NC	+5V _{DC} if Port1 is Host port else not connected	
3	Data1-	Balanced Data Line– Port0	
4	Data2-	Balanced Data Line– Port1	
5	Data1+	Balanced Data Line+ Port0	
6	Data2+	Balanced Data Line+ Port1	
7	GND	Cable Ground Port0	
8	GND	Cable Ground Port1	
9	NC	Not connected	
10	NC	Not connected	

Table 3.4.1 J1 USB connector

3.4.2 J2 – Serial 0 Header connector

If necessary serial port 0 could be used as full modem port via an assembly option. But then you lose the other two serial ports, please contact MPL for further information.

Male header connector 2x5pin, 2mm pitch.
 Type: Samtec TMM-105-02-L-D
 Counterpart: Samtec Type SQT

Serial port 0 is a RS232 interface.

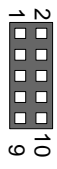
Number	Signal	Description	Pinout
1	NC	not connected	
2	NC	not connected	
3	RXD0	Receive data	
4	RTS0	Request to send	
5	TXD0	Transmit data	
6	CTS0	Clear to send	
7	NC	not connected	
8	NC	not connected	
9	GND	Ground	
10	EARTH	Shield	

Table 3.4.2 J2 Serial0 Header connector

3.4.3 J3 – Serial1/2 Header connector

The user has the option ether to have two serial ports (1 & 2) without handshake signals or one serial port (1) with handshake signals (RTS/CTS) available at this connector. The selection is done through SW usage of the S3C2410 internal UART-registers.

Male header connector 2x5pin, 2mm pitch.
 Type: Samtec TMM-105-02-L-D
 Counterpart: Samtec Type SQT

Serial port 1 and serial port 2 are RS232 interfaces.

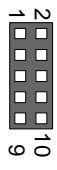
Number	Signal	Description	Pinout
1	NC	not connected	
2	NC	not connected	
3	RXD1	Receive data port 1	
4	RTS1/TXD2	Request to send port 1 or Transmit data port 2	
5	TXD1	Transmit data port 1	
6	CTS1/RXD2	Clear to send port 1 or Receive data port 2	
7	NC	not connected	
8	NC	not connected	
9	GND	Ground	
10	EARTH	Shield	

Table 3.4.3 J3 Serial1/2 Header connector

Note: If serial port 2 is not used, the pins work as handshake signals for serial port 1.

3.4.4 J4 – 10Base-T Header connector

Male header connector 2x6pin, 2mm pitch.
 Type: Samtec TMM-106-02-L-D
 Counterpart: Samtec Type SQT


Number	Signal	Description	Pinout
1	TX+	Transmit Data +	
2	TX-	Transmit Data -	
3	RX+	Receive Data +	
4	NC	not connected	
5	NC	not connected	
6	RX-	Receive Data -	
7	NC	not connected	
8	NC	not connected	
9	NC	not connected	
10	NC	not connected	
11	EARTH	Shield	
12	EARTH	Shield	

Table 3.4.4 J4 10Base-T Header connector

3.4.5 J5 – CAN Header connector

Male header connector 2x5pin, 2mm pitch.
 Type: Samtec TMM-105-02-L-D
 Counterpart: Samtec Type SQT

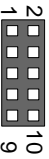
Number	Signal	Description	Pinout
1	NC	not connected	
2	CAN_PWR-	External negative supply voltage input (GND)	
3	CAN_L	CAN_L bus line (dominant low)	
4	CAN_H	CAN_H bus line (dominant high)	
5	CAN_PWR-	External neg. supply voltage input (GND)	
6	NC	not connected	
7	NC	not connected	
8	CAN_PWR+	External pos. supply voltage input (+9..18V _{DC})	
9	EARTH	Shield	
10	EARTH	Shield	

Table 3.4.5 J5 CAN Header connector

Note:

The CAN interface is opto isolated toward all onboard voltages. Therefore an external supply voltage (9V .. 18V_{DC}, 100 mA) is necessary to operate the CAN (connected between pin 8 and 2 of J5)!

3.4.6 J6 – Special Ethernet connector

Female connector 3x1pin, 2mm pitch.
 Type: Samtec SQT-103-01-x-S
 Counterpart: Samtec Type TMM

(Spezial connector for additional Ethernet signals – not mounted on normal board)


Number	Signal	Description	Pinout
1	NIC WAKEUP#	low active wakeup signal in power safe mode	
2	NIC SLEEP#	set Ethernt controller in power safe mode	
3	NIC GPO	general output pin from ethernet controller	

Table 3.4.6 J6 Special Ethernet connector

3.4.7 J7 – Special Clock connector

Female connector 2x1pin, 2mm pitch.

Type: Samtec SQT-102-01-x-S

Counterpart: Samtec Type TMM

(Spezial connector for external CPU clock signal – not mounted on normal board)


Number	Signal	Description	Pinout
1	EXTCLK	External clock signal for CPU	2  1
2	GND	Ground	

Table 3.4.7 J7 Special Clock connector

3.4.8 J8 – Debug / JTAG connector

Male header connector 2x6pin, 2.54mm pitch.

Type: Samtec TSM-106-04-L-DV

Counterpart: Samtec Type HLE, SLW, CES


Number	Signal	Pinout
1	+3.3V	
2	GND	
3	JTAG TRST# CPU	
4	GND	
5	JTAG TDI EPLD/CPU	
6	JTAG TMS EPLD	
7	JTAG TMS CPU	
8	JTAG TCK EPLD	
9	JTAG TCK CPU	
10	JTAG TDO EPLD	
11	JTAG TDO CDU	
12	Reset#	

Table 3.4.8 J8 Debug/JTAG connector

3.4.9 J9 – Special SEC TFT connector

Female connector 3x1pin, 2mm pitch.

Type: Samtec SQT-103-01-x-S

Counterpart: Samtec Type TMM

(Spezial connector for Samsung Electronic Company TFT Display – not mounted on normal board)


Number	Signal	Description	Pinout
1	LCDVF0 / GPC5	Timing control signal for specific TFT (OE)	3  1
2	LCDVF1 / GPC6	Timing control signal for specific TFT (REV)	
3	LCDVF2 / GPC7	Timing control signal for specific TFT (REVB)	

Table 3.4.9 J9 Special SEC TFT connector

3.4.10 J10 – Power, I2C & SPI connector

No other inputs than the pins D3 / E3 together with D2 / E2 must be used to power the board. The board has to be powered with +5V_{DC} and needs typical 200mA current.

Female connector 5x3pin, 2mm pitch.

Type: Samtec YTS-103-01-F-5

Counterpart: Samtec Type TMM, YTT, YTW


Number	Row A	Row B	Row C	Row D	Row E	Pinout
3	+1.8V alive	SYSRST#	PBR#	PWR+ (+5Vin)	PWR+ (+5Vin)	
2	VCC_BATT(+1.8V)	I2C_DATA	I2C_CLK	PWR- (GND)	PWR- (GND)	
1	SPI_SS1#	SPI_MISO1	SPI_MOSI1	SPI_CLK1	GND	

Table 3.4.10 J10 Power, I2C & SPI connector

Note:

- Pin C3 'PBR#' is an input signal, see capture 3.4.10.1.
- Pin A2 'VCC_BATT' is an input power signal, see capture 3.4.10.2.
- Pin A1 '+1.8V alive' can be used as input power signal, see capture 3.4.10.3.
- Pin B3 'SYSRST#' is the open drain output signal of the active low system reset.

WARNING

Be aware of the input power voltage and polarization!

Wrong input power voltage and/or polarization can cause serious damage to the VCMA9 and attached peripherals!

3.4.10.1 Mounting an external push button reset

On the 'Push Button Reset' input (PBR# - J10 pin C3) exists the possibility to mount an external push button for generating a system reset, see

Figure 3-2. The PBR# input is active low and has onboard a 10kΩ pull-up resistor to 3.3V.

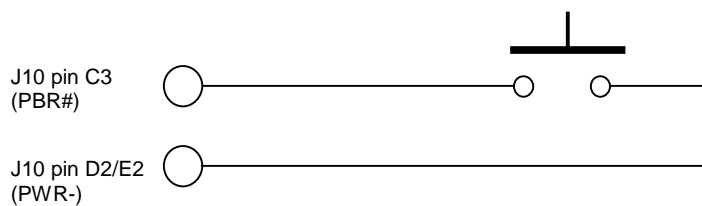


Figure 3-2 Mounting an external Push Button Reset

WARNING

Do not apply other voltages than PWR- or tristate to the PBR# input!

Exceeding these limits can cause serious damage to the VCMA9!

3.4.10.2 Mounting an external battery for RTC backup

On the battery input (VCC_BATT - J10 pin A2) exists the possibility to mount an external battery for RTC backup, see Figure 3-3. This input power pin is only connected to the RTC-power pin of the microprocessor. During power-on state the RTC-power is supplied via the onboard generated +1.8V power supply. If used a voltage of +1.8V has to be connected during power off.

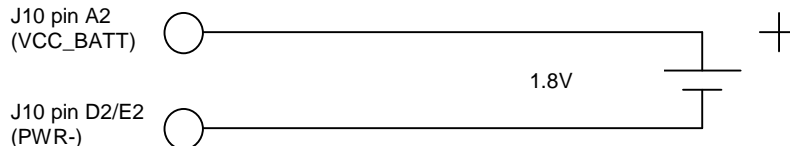


Figure 3-3 Mounting an external RTC-battery

WARNING

**Do not apply higher voltages than +1.8V to VCC_BAT input!
Exceeding these limits can cause serious damage to the VCMA9!**

3.4.10.3 Reaching lowest power consumption with an external 1.8V power supply

If you want get the full advantage of all power management modes, including reaching the lowest power consumption in 'Power-OFF' mode, this option may be useful for you. Over the '+1.8V alive' input (J10 pin A3) you have the possibility to connect an external +1.8V power supply that powers (holds alive) the VCMA9 in the 'Power-OFF' mode. So it is possible to suspend (switch off) the onboard 1.8V power supply and to reduce power consumption of the VCMA9 even more. Before you can use this feature some hardware assembly is necessary, please contact MPL for detailed information!

ATTENTION

**To use this feature hardware assembly is necessary!
Please contact MPL for further information.**

**Do NOT just connect a +1.8V power supply to J10 pin A3.
Take no notice of that can cause serious damage to the VCMA9 and attached peripherals!**

WARNING

**Do not apply other voltages than +1.8V to the '+1.8V alive' input!
Exceeding these limits can cause serious damage to the VCMA9!**

3.4.11 J11 – Digital IO connector

Female connector 5x2pin, 2mm pitch.
 Type: Samtec YTS-102-01-F-5
 Counterpart: Samtec Type TMM, YTT, YTW


Number	Row A	Row B	Row C	Row D	Row E	Pinout
2	GND	DIO_GPF6	DIO_GPF4	DIO_GPF2	DIO_GPF0	 ABCDE
1	DIO_GPF7	DIO_GPF5	DIO_GPF3	DIO_GPF1	+3.3V	

Table 3.4.11 J11 Digital IO connector

Note: Digital IO's are 3.3V interfaces with 5V tolerant input buffers. Onboard all DIO's have a 220 Ohm serie resistor and after power up the inputs are configured to have an internal pull up resistor.

3.4.12 J12 – Analog IO connector

Female connector 5x4pin, 2mm pitch.
 Type: Samtec YTS-104-01-F-5
 Counterpart: Samtec Type TMM, YTT, YTW

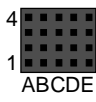
Number	Row A	Row B	Row C	Row D	Row E	Pinout
4	GND	AO_3	AO_2	AO_1	AO_0	 ABCDE
3	GND	AO_REFL	+3.3V	AO_REFH	+5V	
2	GND	AI_3	AI_2	AI_1	AI_0	
1	AI_Vref	AI_7 (Touch XP)	AI_6	AI_5 (Touch YP)	AI_4	

Table 3.4.12 J12 Analog IO connector

Note: Analog input range is from GND to +3.3V. Analog output range depends on settings of switch S1.

3.4.13 J13 – I2S, SD & Timer connector

Female connector 5x4pin, 2mm pitch.
 Type: Samtec YTS-104-01-F-5
 Counterpart: Samtec Type TMM, YTT, YTW

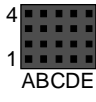
Number	Row A	Row B	Row C	Row D	Row E	Pinout
4	TMRIN_CLK0	TMR_OUT3	TMR_OUT2	TMR_OUT1	TMR_OUT0	 ABCDE
3	TMRIN_CLK1	SD_DATA3	GND	SD_CMD	SD_CLK	
2	SD_DATA2	SD_DATA1	SD_DATA0	+3.3V	GND	
1	I2S_SDO	I2S_SDI	I2S_CDCLK	I2S_SCLK	I2S_LRCK	

Table 3.4.13 J13 I2S, SD & Timer connector

Note: All I2S, SD and Timer signals can be used as DIO's. All signals are 3.3V interfaces with 5V tolerant input buffers.

3.4.14 J14 – LCD & Touch connector

Female connector 5x8pin, 2mm pitch.

Type: Samtec YTS-108-01-F-5

Counterpart: Samtec Type TMM, YTT, YTW

- Normally these pins are used for LCD & Touch interface. Then the pinout of the connector is as follows:

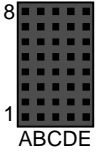
Number	Row A	Row B	Row C	Row D	Row E	Pinout
8	LCD_DATA23	LCD_DATA15	LCD_DATA7	Touch_XPON#	GND	
7	LCD_DATA22	LCD_DATA14	LCD_DATA6	Touch_XMON	LCD_PWREN	
6	LCD_DATA21	LCD_DATA13	LCD_DATA5	Touch_YPON#	LCD_GPC5	
5	LCD_DATA20	LCD_DATA12	LCD_DATA4	Touch_YMON	LCD_DE	
4	LCD_DATA19	LCD_DATA11	LCD_DATA3	+3.3V	LCD_VSYNC	
3	LCD_DATA18	LCD_DATA10	LCD_DATA2	GND	LCD_HSYNC	
2	LCD_DATA17	LCD_DATA9	LCD_DATA1	GND	LCD_CLK	
1	LCD_DATA16	LCD_DATA8	LCD_DATA0	VCC_LCD	LCD_LEND	

Table 3.4.14 J14 As LCD & Touch interface connector

Note: VCC_LCD can be chosen through switch S2 to be +3.3V or +5V.

Note: From production revision [C] on LCD_PWREN has an 10k pull down resistor attached!

- If no LCD & Touch is used, the pins can be used as digital IO's. Then following pinout is given:

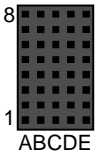
Number	Row A	Row B	Row C	Row D	Row E	Pinout
8	GPD15	GPD7	GPC15	GPG13/EINT21	GND	
7	GPD14	GPD6	GPC14	GPG12/EINT20	GPG4/EINT12	
6	GPD13	GPD5	GPC13	GPG15/EINT23	GPC5	
5	GPD12	GPD4	GPC12	GPG14/EINT22	GPC4	
4	GPD11	GPD3	GPC11	+3.3V	GPC3	
3	GPD10	GPD2	GPC10	GND	GPC2	
2	GPD9	GPD1	GPC9	GND	GPC1	
1	GPD8	GPD0	GPC8	VCC_DIO	GPC0	

Table 3.4.15 J14 LCD & Touch connector

Note: VCC_DIO can be chosen through switch S2 to be +3.3V or +5V.

ATTENTION

Configuration for 'LCD & Touch' or 'digital IO's' has to be done in the S3C2410 internal registers (as example GPCCON register).

Before you can use any signal on this connector, the buffers that drive these signals have to be enabled/configured via extension register GPCD!

CAUTION:

On all VCMA9 up to production revision number [B] the signal LCD_PWREN does NOT have an external pull down resistor! On power up the signal is configured as input and the level is not defined! This floating level can cause serious damage to an attached display.

We recommend you to connect a 10k pull down resistor to the 'Power Enable Pin' of your display!

3.4.15 J15 – Expansion Bus connector

Female connector 5x16pin, 2mm pitch.

Type: Samtec YTS-116-01-F-5

Counterpart: Samtec Type TMM, YTT, YTW

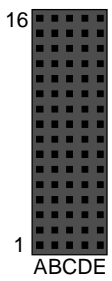
Number	Row A	Row B	Row C	Row D	Row E	Pinout
16	DATA31	DATA15	SYSRST#	XBACK#	ADDR15	
15	DATA30	DATA14	GCS0# or GCS1#	XBREQ#	ADDR14	
14	DATA29	DATA13	GCS2#	EINT17	ADDR13	
13	DATA28	DATA12	GCS3#	EINT16	ADDR12	
12	DATA27	DATA11	XDACK1#	EINT8	ADDR11	
11	DATA26	DATA10	XDREQ1#	ADDR26	ADDR10	
10	DATA25	DATA9	OE#	ADDR25	ADDR9	
9	DATA24	DATA8	WE#	ADDR24	ADDR8	
8	DATA23	DATA7	BE3#	ADDR23	ADDR7	
7	DATA22	DATA6	BE2#	ADDR22	ADDR6	
6	DATA21	DATA5	BE1#	ADDR21	ADDR5	
5	DATA20	DATA4	BE0#	ADDR20	ADDR4	
4	DATA19	DATA3	WAIT#	ADDR19	ADDR3	
3	DATA18	DATA2	+3.3V	ADDR18	ADDR2	
2	DATA17	DATA1	GND	ADDR17	ADDR1	
1	DATA16	DATA0	CPU_CLK	ADDR16	ADDR0	

Table 3.4.16 J15 External Bus connector

Note:

Signal on pin C15 (GCS0# or GCS1#) is selected through switch S3 settings according to following table. Global chipselect 0 (GCS0#) is used for address range from 0x0000 0000h up to 0x0800 0000h (128MB) and GCS1# for 0x1000 0000h until 0x1800 0000h. GCS0# is used as boot chipselect unless NAND-boot is selected (S3-7 on)!

S3-7	S3-8	J15 pin C15	Comment
Off	Off	GCS1#	Boot from onboard NOR-Flash via GCS0#. GCS1# is mapped to Expansion Bus connector for an additional external device.
Off	On	GCS0#	Boot via GCS0# from an external 16 databits wide device connected to Expansion Bus connector. GCS1# is mapped to onboard NOR-Flash.
On	Off	GCS1#	Boot from onboard NAND-Flash (in this mode GCS0# is not used/available). GCS1# is mapped to Expansion Bus connector and onboard NOR-Flash. (Usefull if NOR-Flash not equipped or to double size of NOR-Flash (onboard Flash uses D0 to d15))
On	On	GCS0# (not used in this mode)	Boot from onboard NAND-Flash (in this mode GCS0# is not used/available). GCS1# is mapped to onboard NOR-Flash and GCS0# to Expansion Bus connector, but this chipselect can not be used!

Table 3.4.17 Selected signal on J15 pin C15

4. Operation

4.1 Block diagram

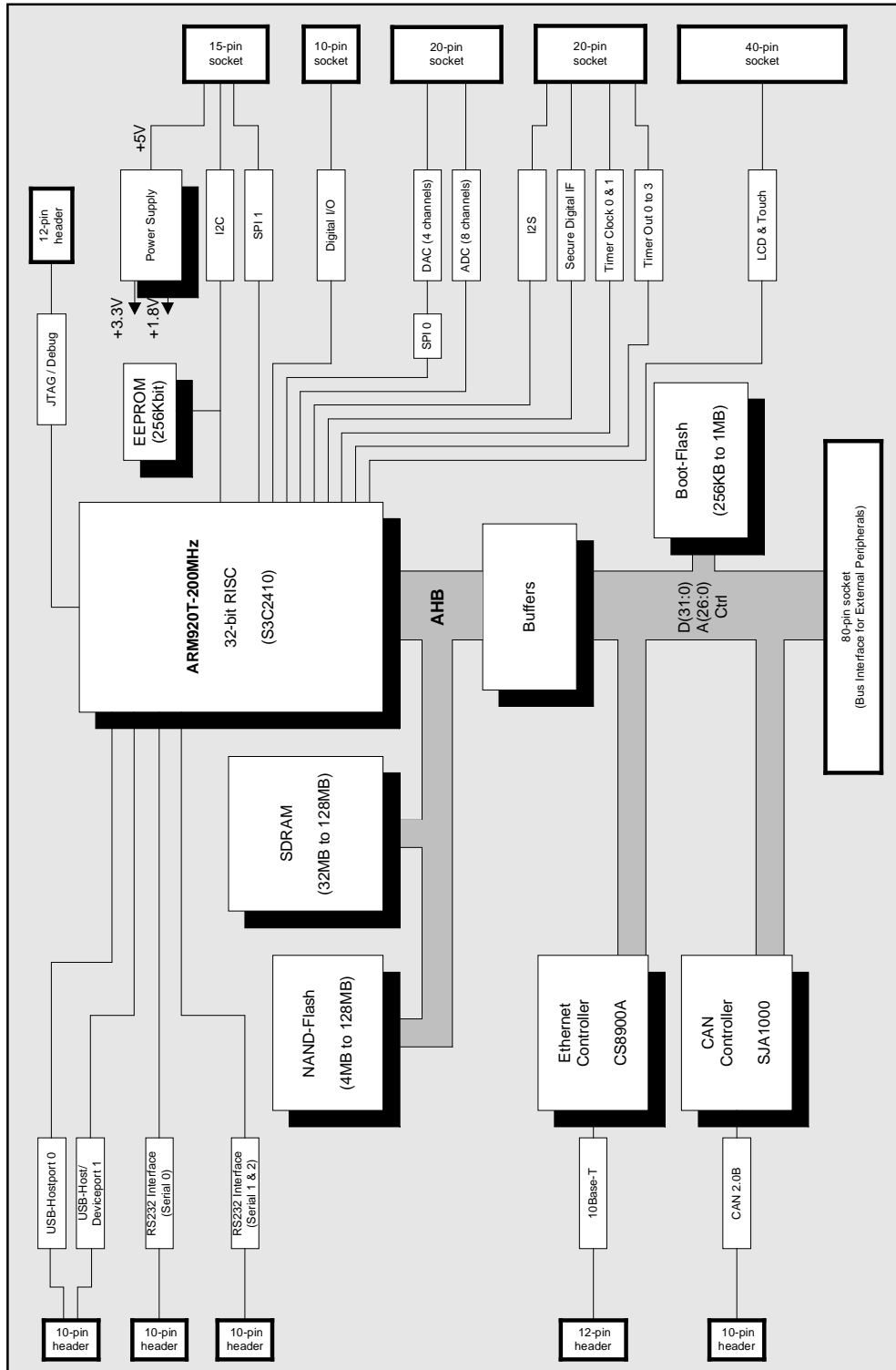


Figure 4.1.1 VCMA9 Block Diagram

4.2 Memory Controller

The memory controller included in the CPU (S3C2410) provides memory control signals required for external memory access. It has the following features:

- Address space: 128Mbytes per bank (total 8 banks giving a total memory space of 1GB)
- Programmable access size (8/16/32-bit) for all banks except bank0 (16-bit ,boot-bank')
- Total 8 memory banks:
 - Six memory banks for ROM, SRAM, etc. (bank0 to bank5)
 - Remaining two banks for main memory (on VCMA9 bank6 is used for the SDRAM; bank7 is not used)
- Programmable access cycles for all memory banks
- External wait to extend the bus cycles
- Supporting self-refresh and power down mode in SDRAM
- Little/Big endian selectable by a software

After Reset the VCMA9 has the following Memory mapping:

Booting from:	Boot ROM	NAND-Flash	
0xFFFF FFFF 0x6000 0000	Not used	Not used	
0x4800 0000	S3C2410 Functional Register Area	S3C2410 Functional Register Area	384MB CPU internal Registers
	Not used		
0x4000 0FFF 0x4000 0000	Internal SRAM (4kB)	Not used	128MB
0x3800 0000	SDRAM (GCS7#)	SDRAM (GCS7#)	128MB Not used on VCMA9!
0x3000 0000	SDRAM (GCS6#)	SDRAM (GCS6#)	128MB Soldered SDRAM on VCMA9
0x2800 0000	CAN/PLD (GCS5#)	CAN/PLD (GCS5#)	128MB PLD-Adr: 0x2800 0100 CAN-Adr: 0x2800 0000
0x2000 0000	Ethernet (GCS4#)	Ethernet (GCS4#)	128MB high 64MB for MEM-Area low 64MB for IO-Area
0x1800 0000	Expansion Bus (EB) (GCS3#)	Expansion Bus (EB) (GCS3#)	128MB
0x1000 0000	Expansion Bus (EB) (GCS2#)	Expansion Bus (EB) (GCS2#)	128MB
0x0800 0000	NOR-Flash or EB (GCS1#)	NOR-Flash or EB (GCS1#)	128MB
0x0000 0FFF 0x0000 0000	NOR-Flash or EB (GCS0#)	<div style="text-align: center; color: green;">Not used</div> Internal BootSRAM (4Kbytes)	128MB

Table 4.2.1 Memory Mapping on VCMA9

If the VCMA9 starts from NAND-Flash or not depends on the DIP-switch S3 settings, according to the following table. Also the device mapping of GCS0# and GCS1# is depending on this settings.

S3-7 NAND boot	S3-8 Boot from EB	Exp. Bus Pin C15	NOR-Flash chipselect	Comment
Off	Off	GCS1#	GCS0#	Boot from onboard NOR-Flash. GCS1# is mapped to Expansion Bus connector.
Off	On	GCS0#	GCS1#	Boot from device on Expansion Bus connector (16bit). GCS1# is mapped to onboard NOR-Flash.
On	Off	GCS1#	GCS1#	Boot from onboard NAND-Flash. GCS1# mapped to both Expansion Bus and NOR-Flash. (NOR-Flash uses D0 to D15)
On	On	GCS0# (not used in this mode)	GCS1#	Boot from onboard NAND-Flash. GCS1# is mapped to onboard NOR-Flash. Expansion Bus connector pin C15 can not be used!

Table 4.2.2 Selected signal on J15 pin C15

4.3 NAND-Flash Controller

The NAND-flash device soldered on the VCMA9 is thought as mass storage device. It is accessed via the NAND-flash controller included in the CPU.

Additional it is possible to load the boot code directly from this onboard NAND-flash. In order to support a NAND-flash boot loader, the S3C2410 is equipped with an internal SRAM buffer called 'Steppingstone'. So when booting from NAND-Flash is selected, the first 4 KBytes of the NAND flash memory will be loaded into Steppingstone and the boot code loaded into Steppingstone will be executed. Generally, the boot code will copy NAND flash content to SDRAM. Using hardware ECC, the NAND flash data validity will be checked. Upon the completion of the copy, the main program will be executed on the SDRAM.

Features of the NAND-Flash controller:

- NAND Flash mode: Support read/erase/program NAND flash memory
- Auto boot mode: The boot code is transferred into Steppingstone during reset. After the transfer, the boot code will be executed on the Steepingstone.
- Hardware ECC detecting block (for hardware detecting and software correcting)
- The Steepingstone 4-KB internal SRAM buffer can be used for another purpose after NAND flash booting.

4.4 Interrupt Controller

The interrupt controller in the S3C2410 receives the request from 56 interrupt sources. These interrupt sources are provided by internal and external peripherals (1 Watchdog-timer, 5 timers, 9 UARTs, 4 DMA, 2 RTC, 2 ADC, 1 IIC, 2 SPI, 1 SDI, 2 USB, 2 LCD, 1 Battery-Fault and max. 24 external interrupts (EINTs)). Some of these interrupt sources, the UARTn and EINTx interrupts are 'OR'ed to the interrupt controller, so that the controller only 32 'directly-wired' interrupts has. The external interrupt request pins (EINTx) can be used as Level- or Edge sensitive interrupt. The polarity of edge and level can be programmed.

When receiving multiple interrupt requests from internal peripherals and external interrupt request pins, the interrupt controller requests FIQ or IRQ interrupt of the ARM920T core after the arbitration procedure. The arbitration procedure depends on the hardware priority logic and the result is written to the interrupt pending register, which helps users notify which interrupt is generated out of various interrupt sources.

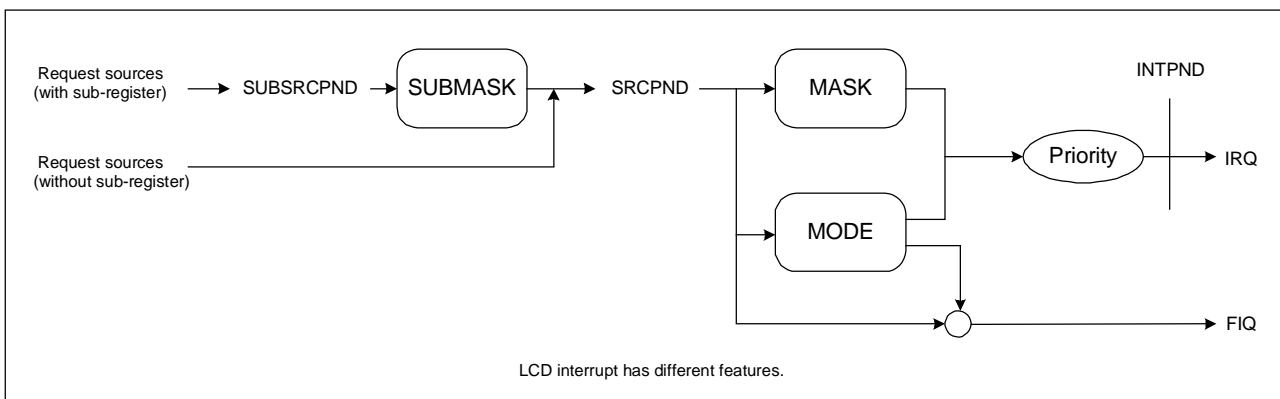


Figure 4.4.1 Interrupt Process Diagram

4.4.1 Interrupt Mode

The ARM920T has two types of Interrupt mode: Fast Interrupt Request (FIQ) or normal Interrupt Request (IRQ). For all interrupt sources the user can determine which mode is used at interrupt request.

F-bit and I-bit of Program Status Register (PSR)

If the F-bit of PSR in ARM920T CPU is set to 1, the CPU does not accept the Fast Interrupt Request (FIQ) from the interrupt controller. Likewise, If I-bit of the PSR is set to 1, the CPU does not accept the Interrupt Request (IRQ) from the interrupt controller. So, the interrupt controller can receive interrupts by clearing F-bit or I-bit of the PSR to 0 and setting the corresponding bit of INTMSK to 0.

4.4.2 Interrupt Pending Register

The S3C2410X01 has two interrupt pending registers: source pending register (SRCPND) and interrupt pending register (INTPND). These pending registers indicate whether or not an interrupt request is pending. When the interrupt sources request interrupt service, the corresponding bits of SRCPND register are set to 1, and at the same time, only one bit of the INTPND register is set to 1 automatically after arbitration procedure. If interrupts are masked, the corresponding bits of the SRCPND register are set to 1. This does not cause the bit of INTPND register changed. When a pending bit of the INTPND register is set, the interrupt service routine starts whenever the I-flag or F-flag is cleared to 0. The SRCPND and INTPND registers can be read and written, so the service routine must clear the pending condition by writing a 1 to the corresponding bit in the SRCPND register first and then clear the pending condition in the INTPND registers by using the same method.

4.4.3 Interrupt Mask Register

This register indicates that an interrupt has been disabled if the corresponding mask bit is set to 1. If an interrupt mask bit of INTMSK is 0, the interrupt will be serviced normally. If the corresponding mask bit is 1 and the interrupt is generated, the source pending bit will be set.

4.4.4 Interrupt Sources

The S3C2410 provides 56 Interrupt sources as seen above. Some of these interrupt sources, as example the three different UART0 interrupts, are 'OR'ed to the interrupt controller, so that the controller only 32 ,directly-wired' interrupts has.

The priority of these interrupts is managed through the priority logic for this 32 interrupt requests. It is composed of seven rotation based arbiters: six first-level arbiters and one second-level arbiter as shown in the figure below:

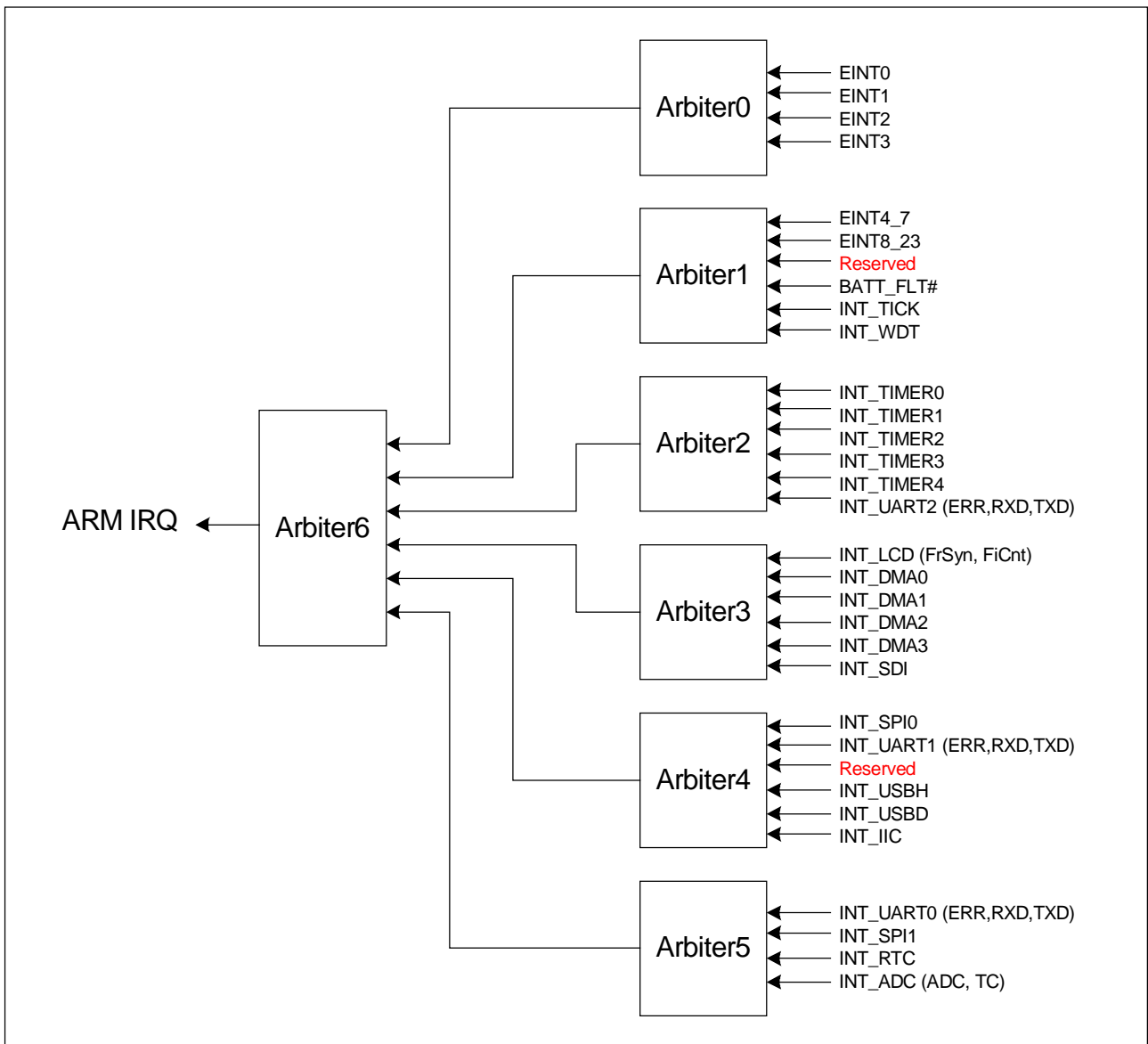


Figure 4.4.2 Interrupt Priority Block

4.4.5 Mapping of external IRQ pins

On the VCMA9 the external interrupt request pins (EINTx) of the CPU are used as follows:

IRQs	Device / Connector	Remarks
EINT0	J11 Pin E2 - Digital IO connector	Multiplexed Pin: normally used as GPF0 for digital IO
EINT1	J11 Pin D1 - Digital IO connector	Multiplexed Pin: normally used as GPF1 for digital IO
EINT2	J11 Pin D2 - Digital IO connector	Multiplexed Pin: normally used as GPF2 for digital IO
EINT3	J11 Pin C1 - Digital IO connector	Multiplexed Pin: normally used as GPF3 for digital IO
EINT4	J11 Pin C2 - Digital IO connector	Multiplexed Pin: normally used as GPF4 for digital IO
EINT5	J11 Pin B1 - Digital IO connector	Multiplexed Pin: normally used as GPF5 for digital IO
EINT6	J11 Pin B2 - Digital IO connector	Multiplexed Pin: normally used as GPF6 for digital IO
EINT7	J11 Pin A1 - Digital IO connector	Multiplexed Pin: normally used as GPF7 for digital IO
EINT8	J16 Pin D12 – Expansion bus connector	for additional devices connected to the expansion bus
EINT9	CAN_IRQ#	mapped to low active onboard CAN device interrupt
EINT10	not accessible	Multiplexed Pin: used as 'SPI_SS0#' on the VCMA9
EINT11	J10 Pin A1 - Power, I2C & SPI connector	Multiplexed Pin: normally used as SPI_SS1# for SPI channel 1
EINT12	not accessible	Multiplexed Pin: used as 'LCD Power Enable' or GPG4 on the VCMA9
EINT13	J10 Pin B1 - Power, I2C & SPI connector	Multiplexed Pin: normally used as SPI_MISO1# for SPI channel 1
EINT14	J10 Pin C1 - Power, I2C & SPI connector	Multiplexed Pin: normally used as SPI_MOSI1# for SPI channel 1
EINT15	J10 Pin D1 - Power, I2C & SPI connector	Multiplexed Pin: normally used as SPI_CLK1# for SPI channel 1
EINT16	J16 Pin D13 – Expansion bus connector	for additional devices connected to the expansion bus
EINT17	J16 Pin D14 – Expansion bus connector	for additional devices connected to the expansion bus
EINT18	Ethernet_IRQ	mapped to high active onboard Ethernet device interrupt
EINT19	J13 Pin A3 – I2S, SD & Timer connector	Multiplexed Pin: normally used as TMRIN_CLK1 for PWM Timer
EINT20	J14 PinD7– LCD&Touch connector	Multiplexed Pin: normally used as XMON for Touch Controller
EINT21	J14 PinD8 – LCD&Touch connector	Multiplexed Pin: normally used as XPON# for Touch Controller
EINT22	J14 PinD5 – LCD&Touch connector	Multiplexed Pin: normally used as YMON for Touch Controller
EINT23	J14 PinD6 – LCD&Touch connector	Multiplexed Pin: normally used as YPON# for Touch Controller

Table 4.4.1 External Interrupt mapping

EINT8, EINT16 and EINT17 are mapped to the expansion bus connector and can be used by the user for additional interrupts from external devices.

4.5 DMA Controller

The S3C2410 supports a four-channel DMA controller that is located between the system bus (AHB; also the bus for external devices) and the peripheral bus (APB; CPU internal bus for CPU integrated peripherals). Each channel of the DMA controller can perform data movements between devices in the system bus and/or peripheral bus with no restrictions. In other words, each channel can handle the following four cases:

- 1) both source and destination are in the system bus
- 2) the source is in the system bus while the destination is in the peripheral bus
- 3) the source is in the peripheral bus while the destination is in the system bus
- 4) both source and destination are in the peripheral bus.

The main advantage of the DMA is that it can transfer the data without CPU intervention. The operation of DMA can be initiated by software or requests from internal peripherals or external request pins.

4.5.1 DMA Request Sources

Each channel of the DMA controller can select one DMA request source among five DMA sources if H/W DMA request mode is selected by DCON register. (Note that if S/W request mode is selected, this DMA request sources have no meaning at all.)

DMA-Channel	Source 0	Source 1	Source 2	Source 3	Source 4
0	<i>Ethernet-RX</i>	UART0	SDI	Timer	USB device EP1
1	<i>XDREQ1#</i>	UART1	I2SSSDI	SPI0	USB device EP2
2	I2SSSDO	I2SSDI	SDI	Timer	USB device EP3
3	UART2	SDI	SPI1	Timer	USB device EP4

Table 4.5.1 Possible DMA sources for each channel

XDREQ1# represents an external sources (External Device) connected via expansion bus. I2SSDO and I2SSDI represent IIS transmitting and receiving, respectively.

4.5.2 DMA Operation

DMA uses a three-state FSM (finite state machine) for its operation, which is described below:

- State-1: As an initial state, the DMA waits for a DMA request. If it comes, it goes to state-2. At this state, DMA ACK and INT REQ are 0.
- State-2: In this state, DMA ACK becomes 1 and the counter (CURR_TC) is loaded from DCON[19:0] register. Note that the DMA ACK remains 1 until it is cleared later. Then it goes to state-3.
- State-3: In this state, a sub-FSM handling the atomic operation of DMA is initiated. The sub-FSM reads the data from the source address and then writes it to destination address. In this operation data size, transfer size and service mode are considered. The main FSM (this FSM) counts down the CURR_TC when the sub-FSM finishes each atomic operation and asserts the INT REQ signal when CURR_TC becomes 0 and the interrupt setting of DCON[29] register is set to 1. In addition, it clears DMA ACK if one of the following conditions is met:
- 1) CURR_TC becomes 0 in the Whole service mode
 - 2) Atomic operation finishes in the Single service mode.

Service Modes:

- Single: In this service mode the three states of main FSM are performed. Then DMA operation stops and waits for another DMA REQ. If a new DMA REQ comes in, all three states are repeated. Therefore, DMA ACK is asserted and then deasserted for each atomic transfer.
- Whole: In the Whole service mode, main FSM waits at state-3 until CURR_TC becomes 0. Therefore DMA ACK is asserted during all the transfers and then deasserted when TC reaches 0.

However, INT REQ is asserted only if CURR_TC becomes 0 regardless of the service mode (Single service mode or Whole service mode).

Transfer Size:

DMA holds the bus firmly during the transfer of data. So other bus masters can not get the bus. There are two different transfer sizes:

Unit: One Read and one Write Cycle are done.

Burst 4: Four sequential Reads and Writes are performed.

S3C2410 External DMA DREQ/DACK Protocol

There are three types of external DMA request/acknowledge protocols (Single service Demand, Single service Handshake and Whole service Handshake mode). Each type defines how the signals like DMA request and acknowledge are related to these protocols.

Demand: If XDREQn# remains asserted, the next transfer starts immediately. Otherwise it waits for XDREQn# to be asserted.

Handshake: DMA deasserts XDACKn# after DMA operation is finished and XDREQn# is deasserted! It waits until XDREQn# is deasserted.

CAUTION:

XDREQn# has to be asserted (low) only after the deassertion (high) of XDACKn# !

For further information about DMA-Registers and DMA Timing diagrams please see the S3C2410 User Manual.

4.6 Digital Analog Converter (DAC)

Via Serial Peripheral Interface (SPI) Channel 0 a Digital-to-Analog Converter is connected to the CPU. A MAX5106 DAC with four separate 8-Bit digital-to-analog converters is placed onboard. This Rail-to-Rail DAC has separate High and Low reference inputs (Input range reaching from GND to +5V_{DC}), that are controlled via DIP-Switch1 (see chapter 3.2.1). Furthermore the DAC has nonvolatile internal registers, that allow automatic initialization of the DAC outputs and operating states during power-up! Also it supports a software controlled 10uA shutdown mode and a mute state that drives the DAC outputs to the Low-Reference voltage.

The analog output signals from the DAC are available on the Analog IO connector J12.

Attention:
Be aware that the DAC Reference Input Voltage Range for V_{REFH} and V_{REFL} must be between GND and +5V_{DC}!

4.6.1 DAC Registers

The MAX5106 has ten 8-bit registers: eight DAC data registers (one volatile and nonvolatile for each channel) that hold the DAC output data and two (one volatile and one nonvolatile) mute/shutdown registers that hold the operating state of each channel.

DAC-data register:

Bit in Register	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
8-bit DAC data	x	x	x	x	x	x	x	x

Table 4.6.1 MAX5106 DAC-data register

Mute/Shutdown register:

Bit in Register	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Controlling Function	Mute DAC3	Mute DAC2	Mute DAC1	Mute DAC0	Shutdown DAC3	Shutdown DAC2	Shutdown DAC1	Shutdown DAC0

Table 4.6.2 MAX5106 DAC-operating register

Data can be written to a selected volatile register, immediately updating the DAC output, or can be written to a selected nonvolatile register for storage. The values stored in the nonvolatile registers are loaded at power up into the volatile registers initializing the device!

Volatile Registers:

The volatile registers hold the current, valid value of each DAC. Data is written to these registers in two ways: directly from DIN or loaded from the respective nonvolatile. The volatile registers retain data as long as the device is enabled and powered. Once power is removed or the device is shut down, the volatile registers are cleared.

Nonvolatile Registers:

The nonvolatile registers retain data even after power is removed. On power-up, the power on reset circuitry and internal oscillator control the transfer of data from the nonvolatile registers to the volatile registers, which automatically initializes the device upon startup. Stored data is accessed in two ways: transferring data to a volatile register to update the respective DAC output or reading data through DOUT.

4.6.2 Communication via SPI-0

The Serial Peripheral Interface (SPI) is a serial data transfer interface. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). There are 4 I/O pin signals associated with SPI transfers. For SPI channel 0 following pins of the S3C2410 are used:

Funtion	Signal-Name	Pin on S3C2410	Direction (from S3C2410)	Comment
Clock	SPI_CLK0	P8	Output	Host generates the clock (MAX5106: max. 1MHz)
Data In	SPI_MISO0	T7	Input	(MAX5106: Clk to Dout valid max. 1us)
Data Out	SPI_MOSI0	U7	Output	(MAX5106: Din Setup Time min. 100ns)
Chip Select	SPI_SS0#	T8	Output	Low active signal (MAX5106: CS# Setup Time min. 100ns)

Table 4.6.3 S3C2410 SPI channel 0 interface

The MAX5106 serial interface expects data to be sent MSB first and a correct Command must be transmitted in one 14-bit word. The received serial data is clocked into a 14-bit shift register and should look like follows:

Bit-Nr	14-bit Serial Word													
	13 (MSB)	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Function	Start-bit	Command-bits		Address-bits			Data-bits							
Value	1	C1	C0	A2	A1	A0	x	x	x	x	x	x	x	x

Table 4.6.4 MAX5106 Expected Command-Word

Command-bits:

C1	C0	Function
0	0	Write data to nonvolatile register (Output remains unchanged)
0	1	Write data to volatile register (Update corresponding DAC-Output immediately)
1	0	Read data from nonvolatile register (D7-D0 are ignored on Data-In pin)
1	1	Load content of nonvolatile register into corresponding volatile register and update outputs. (D7-D0 are ignored on Data-In pin)

Table 4.6.5 MAX5106 Meaning of Command-bits

Address-bits:

A2	A1	A0	Function
0	0	0	Data registers for DAC0 (
0	0	1	Data registers for DAC1
0	1	0	Data registers for DAC2
0	1	1	Data registers for DAC3
1	0	0	Mute/Shutdown registers
others			Reserved

Table 4.6.6 MAX5106 Meaning of Address-bits

On the MAX5106 data is clocked in on the rising edge of clock while Chipselect is low (device enabled). Note that clock should be low if it is stopped between updates.

Because the SPI Interface in the S3C2410 always transfers 8-bits, 16-bits will be send to the MAX5106. So we must add two dummy bits at the end of the transfer that the communication with the MAX5106 works! A correct command send to the MAX5106 by the S3C2410 SPI channel 0 has following pattern:

Bit-Nr	16-bit Serial Word																
	15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)	
Function	Start-bit	Command-bits		Address-bits			Data-bits									Dummy-bits	
Value	1	C1	C0	A2	A1	A0	x	x	x	x	x	x	x	x	1	1	

Table 4.6.7 DAC-Command pattern to be send by S3C2410

4.7 Connecting a LCD

On the 40-pin 2mm socket J14 all LCD signals are available to connect a display. The LCD controller in the S3C2410 supports monochrome or color STN LCD as well as a color TFT LCD. Also multiple screen sizes (640x480, 320x240, 160x160 and others) are supported. For TFT LCD displays a maximum of 16M colors (24 bit per pixel) are possible. For STN LCD displays monochrome, 4 or 16 gray levels as well as 256 or 4096 colors are possible.

MPL tested the interface with a 6.4" color VGA TFT display from LG. For further information about this display and the connection please contact MPL.

Finally before connecting any display to the VCMA9 the user has to adapt the LCD registers according the display requirements to get the necessary signal timing (please see 'S32410X User's Manual' chapter 15 LCD Controller).

WARNING

Be aware to adapt the LCD registers according your display requirements before connecting a display. Wrong LCD register settings may damage your display!

4.8 Connecting a touch

The S3C2410 on the VCMA9 has a touch controller integrated. To use this controller some additional external control logic is necessary. If the touch controller is used, it needs ADC input channel 5 and 7 for measuring the touch signals (X- and Y-position).

MPL tested the interface with the touch model No. G-24-4D-GUN from Gunze (6.5" resistive touch). For further information about this touch and the connection to the VCMA9 please contact MPL.

4.9 Extension registers

The extension registers listed in this section are implemented in the onboard PLD. They are 8 bits wide and mapped to the chip select signal GCS5# from the S3C2410. This chip select has an address space of 128MB and starts at 0x2800 0000h. It is shared with the onboard CAN controller and the lower 256 addresses are used by the CAN device. So the PLD base address is located at 0x2800 0100h.

Offset	Name	Type	Function
6	SDRAM_REG	Read only	Information about onboard SDRAM size
5	BOARD_REG	Read only	Board Revision and populated Configuration
4	GPCD_REG	Read/Write	Ext. buffer control of S3C2410 General Port C and D signals
3	MISC_REG	Read/Write	Miscellaneous Register
2	CAN_REG	Read/Write	CAN Register
1	NIC_REG	Read/Write	Ethernet Register
0	PLD_ID	Read only	PLD code version and revision

Table 4.9.1 Extensions Registers

4.9.1 PLD Register

This register is used to identify the code version and revision of the programmable onboard PLD.

PLD ID				0x2800 0100h				Read only	
	D7	D6	D5	D4	D3	D2	D1	D0	
Read	PLD Version				PLD Revision				
Default	0	0	0	0	0	0	0	0	

Table 4.9.2 PLD_ID register

PLD Version (read)

Binary decoded PLD Version. Currently Version = 0.

PLD Revision (read)

Binary decoded PLD Revision. Currently Revision = 0.

4.9.2 NIC Register

This register is used to control the resetline of the Ethernet controller.

NIC_REG				0x2800 0101h				Read/Write	
	D7	D6	D5	D4	D3	D2	D1	D0	
Read	Reserved							NICRST	
Default	0	0	0	0	0	0	0	0	

Table 4.9.3 NIC Register

NICRST (read/write)

If set the resetline to the Ethernet controller is active – the ethernet chip is hold in the 'Reset-state'.

4.9.3 CAN Register

This register is used to control the resetline of the CAN controller.

CAN_REG				0x2800 0102h				Read/Write	
	D7	D6	D5	D4	D3	D2	D1	D0	
Read	Reserved							CANRST	
Default	0	0	0	0	0	0	0	0	

Table 4.9.4 PLD Partnumber register

CANRST (read/write)

If set the resetline to the CAN controller is active – the CAN chip is hold in the 'Reset-state'.

4.9.4 MISC Register

This register is used to read back the actual switch S3-8 setting and to control the CPU output reset signal 'RSTOUT'.

MISC_REG				0x2800 0103h			Read/Write	
	D7	D6	D5	D4	D3	D2	D1	D0
Read	<i>Boot CS</i>	<i>Reserved</i>					<i>250MHz capable CPU</i>	<i>CPURST Enable</i>
Default	X	0	0	0	0	0	x	0

Table 4.9.5 MISC register

Boot CS (read)

Represents the setting of switch S3-8. If set the switch is off. Meaning the Boot-chipselect is mapped to an onboard device (ether NAND-Flash or Boot-Flash, depending of S3-7). If zero the switch is on and booting from an external device connected to the expansion bus connector is expected.

250MHz capable CPU (read)

Represents if the on board soldered CPU type is capable of running at 250MHz. If zero the CPU soldered on board runs only up to 200 MHz, else if one the CPU supports up to 250MHz CPU clock frequencies.

CPURST Enable (read/write)

If set it is possible to generate a system reset via the RSTOUT-pin of the S3C2410.

4.9.5 GPCD Register

This register is used to control the onboard databuffers connected to the S3C2410 General Port C and D signals. If the LCD controller of the S3C2410 is used, these pins act as LCD interface pins (see capture 3.4.14)! So all bits have to be set to zero.

GPCD_REG				0x2800 0104h			Read/Write	
	D7	D6	D5	D4	D3	D2	D1	D0
Read	<i>Direction GPD8-15</i>	<i>Direction GPD0-7</i>	<i>Direction GPC8-15</i>	<i>Direction GPC0-5 +GPG4</i>	<i>Output Enable GPD8-15</i>	<i>Output Enable GPD0-7</i>	<i>Output Enable GPC8-15</i>	<i>Output Enable GPC0-5 +GPG4</i>
Default	0	0	0	0	1	1	1	1

Table 4.9.6 GPCD register

Direction GPxy (read/write)

These bits directly controls the 'Direction'-signal of the corresponding databuffer. A low level (zero) on the 'Direction'-signal of the databuffer means the buffer is driving the signal coming from the S3C2410 out to the connector J14. So the pins are used as General Port Outputs or as LCD-interface pins.

If set the Databuffer drives the signal from the connector J14 to the S3C2410. So the General Port x pins y can be used as inputs.

Output Enable GPxy (read/write)

These bits directly control the 'Output Enable'-signal of the corresponding databuffer. The 'Output Enable'-signal of the Databuffer is low active, meaning a zero enables the buffer.

4.9.6 BOARD Register

This register is used to get some board information.

BOARD_REG				0x2800 0105h		Read only		
	D7	D6	D5	D4	D3	D2	D1	D0
Read	<i>Reserved</i>		<i>Board Revision</i>		<i>Reserved</i>		<i>HW-Configuration</i>	
Default	0	0	0	0	0	0	x	x

Table 4.9.7 Board register

Board Revision (read)

Binary decoded PCB Revision. Add an ASCII 'A' to this number to get the PCB Revision. Currently Board Revision = 0 => 'A'.

HW-Configuration (read)

Used to distinguish different population or other options. Connected to VCC or GND via 'Config-Resistors'. Currently one population option is valid:

Configuration	Option
00	not defined yet
01	not defined yet
10	not defined yet
11	VCMA9-1 (fully equipped)

Table 4.9.8 HW-Configuration bits

4.9.7 SDRAM Register

This register is used to get information about the onboard soldered SDRAM chips.

SDRAM_REG				0x2800 0106h		Read only		
	D7	D6	D5	D4	D3	D2	D1	D0
Read	<i>Number SDRAM chips</i>				<i>SDRAM architecture</i>			
Default	x	x	x	x	x	x	x	x

Table 4.9.9 Board register

Number SDRAM chips (read)

Shows the actual number of mounted SDRAM chips to setup the memory controller.

Number SDRAM chips	Option
0000	4 SDRAM chips soldered onboard
0001	1 SDRAM chip soldered onboard
0010	2 SDRAM chips soldered onboard
others	not defined yet

Table 4.9.10 Number SDRAM chip bits

SDRAM architecture (read)

Shows the actual used SDRAM chip architecture to setup the memory controller.

Configuration	Option
0000	4Mx8x4B $\bar{\text{O}}$ 16M x 8
0001	8Mx8x4B $\bar{\text{O}}$ 32M x 8
0010	2Mx8x4B $\bar{\text{O}}$ 8M x 8
0011	4Mx8x2B $\bar{\text{O}}$ 8M x 8
others	not defined yet

Table 4.9.11 SDRAM architecture bits

5. Support information

5.1 MPL AG

In case of questions contact MPL AG or your local distributor.

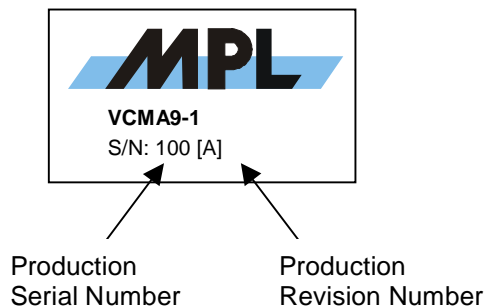
MPL AG homepage: www.mpl.ch
Email address: support@mpl.ch

5.2 Related documents

The high integration level of equipped components offers a lot more features than could possibly be described within the scope of this manual. Several data books related to all the different components are available either directly from the respective manufacturer or distributor or by downloading from the manufacturers Internet site..

5.3 Production serial and revision number

To get the actual production revision number of your device, please see the label on the VCMA9 board.



5.4 VCMA9-Baseboard from MPL

To facilitate the connection to the different connectors on the VCMA9 MPL AG provides a 'Connector-Board' the VCMA9-BB1. So the user just put on this Baseboard to the VCMA9 and all interfaces are available on the usual standard connectors. For more information please contact MPL AG.

6. Appendix

6.1 Mounting VCMA9 as add-on board

The VCMA9 can be directly put up onto a baseboard.

The distance between the two boards depends on the chosen connector counterparts. Please be sure not to use too high distance holders between the two boards so that the connection is guaranteed!

6.2 Power up the VCMA9

Normally on the VCMA9 the U-Boot bootloader is installed. By default this bootloader uses serial line 0 (J2) as its console device. The parameters of this serial communication are as follows by default, but can be changed if necessary:

- 9600 baud
- 8 bits
- parity none
- 1 stop bit
- no handshake

To get in contact with the U-Boot's command interface connect serial line 0 of the VCMA9 with a PC or terminal. There you can use your favorite terminal program (TeraTerm, Minicom, ...).

NOTE

Be aware that you have to use a so called "null modem" or "crossed" cable to get a working communication link!

For further information about the U-Boot bootloader please refer to the 'U-Boot for the VCMA9' User Manual.

Copyright and revision history

Copyright © 2002 by MPL AG Elektronikunternehmen. All rights reserved. Reproduction of this document in part or whole, by any means is prohibited, without written permission from MPL AG Elektronikunternehmen.

This manual reflects production revision A of the VCMA9.
Publication Date: September 2002

Revision Index	Date	Comment
Rev. A	02.09.2002	Created for VCMA9 board revision A - Preliminary
Rev. A1	18.03.2003	Document corrected; LCD and Touch chapter added
Rev. B	23.06.2003	Add chapter 4.9.7 SDRAM Register Add chapter 6.2 Power up the VCMA9 Remark to S3-1 (3.2.3) Remark to CAN interface (3.4.5)
Rev. C	06.08.2004	Error corrected in chapter 4.9.5 bit D0 and D4 are valid for GPC0-5 + GPG4 Chapter 1.1 MEH-number of U-Boot Manual added New bit added in MISC register for identification of faster CPU's (chapter 4.9.4)

Disclaimer

The information contained herein is believed to be accurate as of the date of this publication, however, MPL AG will not be liable for any damages, including indirect or consequential, arising out of the application or use of any product, circuit or software described herein.

MPL AG reserves the right to make changes to any product herein to improve reliability, function or design at any time.

Trademarks

Brand or product names are trademarks and registered trademarks of their respective holders.

Our local distributor: