

HIGH PERFORMANCE CMOS 68332 VERSATILE COMPUTER MODULE

The VCM332B/D is one of the most powerful single board computers, in relation to its physical size, available on the market today. Built around the popular MC68332 microprocessor from Motorola and operating at up to 25.17MHz, this module contains a maximum of 1M byte of battery backed SRAM, 1M byte of FLASH-ROM, 512K byte of EPROM, 1K bit serial EEPROM, three serial ports and a Real Time Clock. Board dimensions are kept to a minimum which results in a size of just 95x69mm.

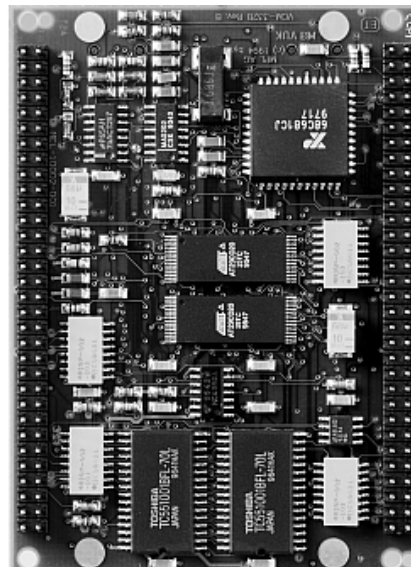
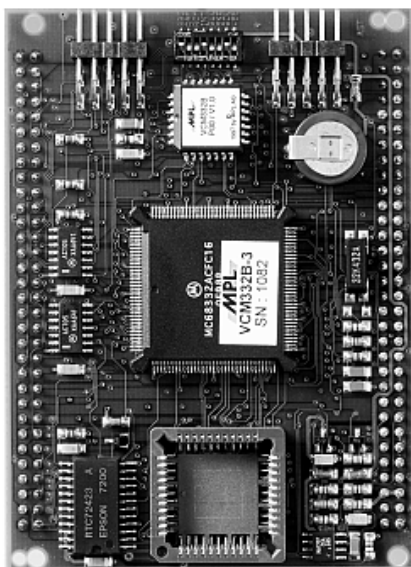
The board is configurable by the use of dip switches and contains connectors for debugger and serial interfaces. Connection to the board is made through two 64-pin connectors. Almost all signals of the MC68332 and peripherals are available on these connectors.

The use of 100% CMOS technology results in an exceptionally low power consumption of just 140mA at 5V (with 256K byte SRAM, 128K byte EPROM on board operating at 16.78MHz).

With its compact design and economic price the VCM332B/D is an ideal solution for many industrial applications requiring high performance processing power in a small cost effective package.

TECHNICAL FEATURES

- High performance MC68332
- Clock programmable from DC to 16.78MHz (VCM332B) or 25.166MHz (VCM332D)
- 256K byte or 1M byte of SRAM included
- SRAM can be battery buffered with an on-board battery
- Up to 1M byte FLASH-ROM which is on-board programmable
- 128K byte or 512K byte EPROM (socket only)
- EPROM must be 16-bit wide in J/PLCC package
- 1024-bit serial EEPROM
- Real Time Clock with calendar
- Background debug interface
- Three serial ports (1x MC68332, 2x 68681 DUART)
- On-board TTL to RS-232 conversion for two ports
- Two connectors which hold all relevant signals
- Configuration dip switch for chip selects, interrupt, battery backup etc.
- Battery undervoltage detection
- All CMOS design
- Compact board dimensions 95 x 69mm
- 6-layer PCB design
- Power consumption +5V /140mA
- Temperature range 0° to 70 °C (+32° to 132 °F)
- Optionally available in extended temp. range -25° to 85 °C



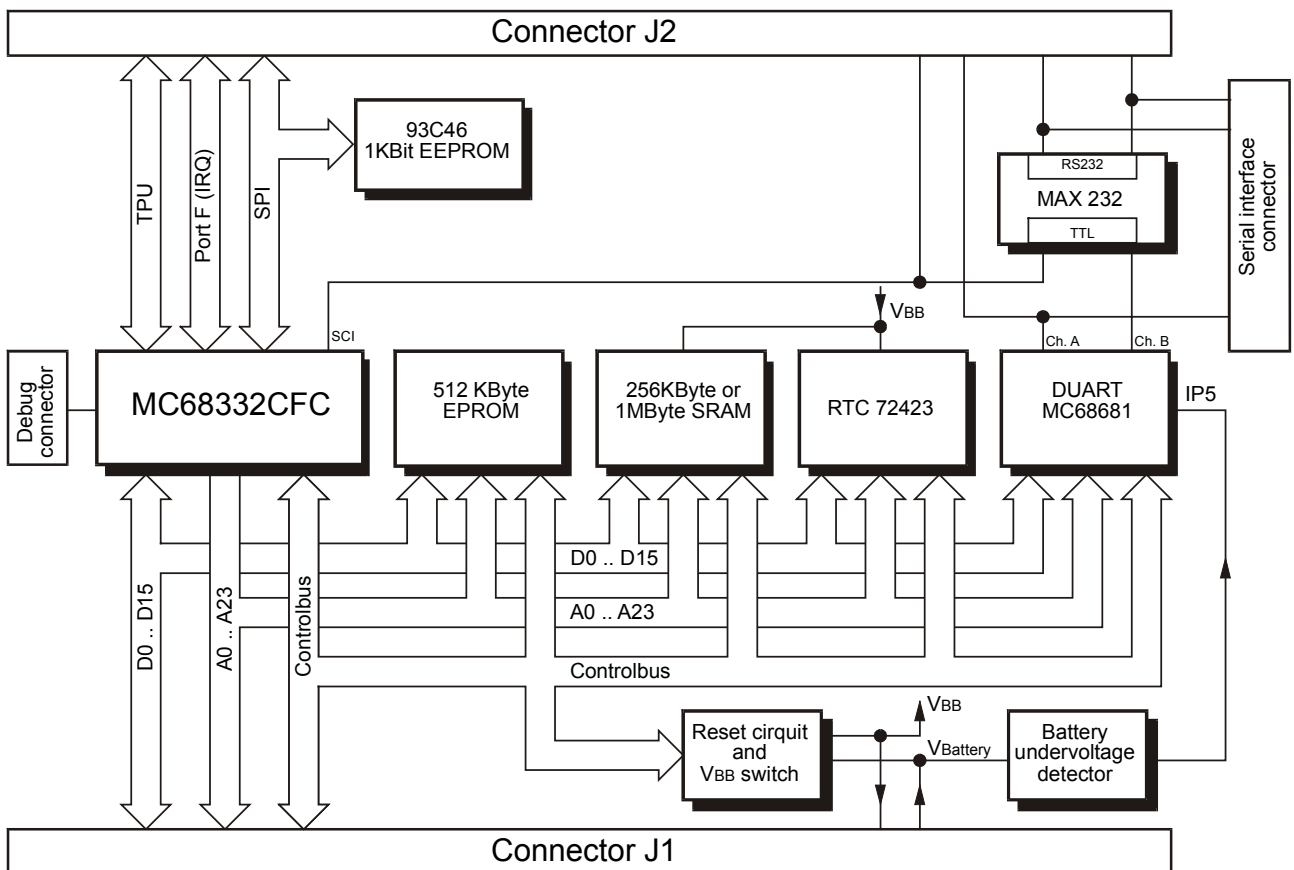
References:

- VCM332B-1: CMOS Versatile computer module 16MHz, 256K byte SRAM, 1M byte FLASH, 0° to 70°C
- VCM332D-1: CMOS Versatile computer module 25MHz, 256K byte SRAM, 1M byte FLASH, 0° to 70°C
- VCM332B-2: CMOS Versatile computer module 16MHz, 1M byte SRAM, 1M byte FLASH, 0° to 70°C
- VCM332D-2: CMOS Versatile computer module 25MHz, 1M byte SRAM, 1M byte FLASH, 0° to 70°C
Extended temperature range (-25° to 85°C) on request

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VCM332B Block diagram

1. INTRODUCTION

1.1 SAFETY PRECAUTIONS AND HANDLING

For personal safety and safe operation of the VCM332, follow all safety procedures here and in other sections of the manual.

- Power must be removed from the system before installing (or removing) the VCM332 to prevent the possibility of personal injury (electrical shock) and/or damage to the product.
- Handle the product carefully, i.e. dropping or mishandling the VCM332 can cause damage to assemblies and components.
- Do not expose the equipment to moisture

WARNING

There are no user-serviceable components on the VCM332!

1.2 ELECTROSTATIC DISCHARGE (ESD) PROTECTION

Various electrical components within the product are sensitive to static and electrostatic discharge (ESD). Even a non sensible static discharge can be sufficient to destroy or degrade a component's operation!

Following the precautions listed below will avoid ESD-related problems:

- Use a properly installed anti static pad on your work surface.
- Wear wrist straps and observe proper ESD grounding techniques.
- Leave the unit in its antistatic cover until you are prepared to install it in the desired environment. When it is out of its protective cover, place the unit on the properly grounded anti static work surface pad.
- Do not touch any components on the product. Handle the product by its card edges.

1.3 EQUIPMENT SAFETY

Great care is taken by MPL AG that all it's products are thoroughly and rigorously tested before leaving the factory to ensure that they are fully operational and conform to the specifications given in this manual. However, no matter how reliable a product, there is always the remote possibility that a defect may occur. The occurrence of a defect on this device may, under certain conditions, cause a defect to occur in adjoining and/or connected equipment. It is the users responsibility to ensure that adequate protection for such equipment is incorporated when installing this device. MPL AG accepts no responsibility whatsoever for such kind of defects, however caused.

2. GENERAL INFORMATION

2.1 DESCRIPTION

The VCM332B/D is a powerful and compact single board computer, built in all CMOS low power technology around Motorola's MC68332 operating at up to 25.166MHz.

The MC68332 is a member of the MC68300 family of modular embedded controllers. Its core is the 32-bit instruction processing module (CPU32), based on the powerful MC68020. Also integrated on the chip are intelligent peripheral submodules that dramatically increase functionality: A Time Processing Unit (TPU) with 16 independent channels allows for performing any time-related activities from simple input capture or output compare to complicated motor control. The System Integration Module (SIM) offers programmable chip selects with wait state generators, various monitors (i.e. bus, interrupt, watchdog), a PLL circuit to dynamically change the system speed and a full bus interface (24-bit address/16-bit data). The Queued Serial Module (QSM) contains the well known QSPI with additional chip select lines and a Serial Communication Interface (SCI) that allows for communication with the outside world (e.g. via RS-232). The fast 2 Kbyte SRAM module can be used by the CPU32 or the TPU.

Besides the features of the MC68332, the VCM332B/D is loaded with additional features that make the board even more flexible and versatile. The on-board memory of the VCM332B/D consists of 256K byte SRAM (optional 1M byte), up to 1M byte on-board programmable FLASH-ROM and up to 512K byte of 16-bit wide EPROM (only PLCC/JLCC socket is mounted). A 1024-bit serial access EEPROM allows the permanent storage of useful operating parameters. A DUART 68681 adds two more serial ports to the existing SCI port of the MC68332. Two of these ports are on-board converted to RS-232 levels. Time and date functions are offered by a Real Time Clock. RTC and SRAM can be battery buffered using the on-board battery; except the optional variant of the 25.166MHz VCM332D with zero Wait States SRAM. In this case only the RTC is battery backed due to the relative high current consumption of fast SRAM devices in standby mode. Additionally, an external battery can be connected. All logic necessary for switch-over between batteries and battery undervoltage detection is already provided on-board.

All signals of the MC68332 and the on-board peripherals that do not have a MPL defined purpose, are combined on two 64 pin connectors. Users are free to realize their own adapter-board (e.g. with additional memory and/or I/O's). Some users may wish to use the VCM332B/D together with products based on the G-64/96 bus. For this purpose, MPL AG provides all material necessary for a correct adaptation of the VCM332B/D to the G-64/96 bus (i.e. schematic and programmed EPLD).

Software development on the VCM332B/D is simplified by the availability of the OS-9 real-time, multitasking operating system and the support of debug tools. On the MC68332 a background debugger is implemented in micro code. The VCM332B/D provides a 10 pin connector that interconnects this on-chip debugger with a number of PC-based development tools (e.g. from Abatron or Motorola). In addition, Hewlett-Packard offers in-circuit emulators (HP647xx) and adapters (E3407A) for the MC68332 that can be used on the VCM332B/D.

With its compact design and economic price the VCM332B/D offers the ideal solution for many industrial applications requiring high performance processing power in a small, cost effective package. The low power consumption and small physical size also make it the perfect choice for portable, battery driven products.

2.2 TECHNICAL CHARACTERISTICS

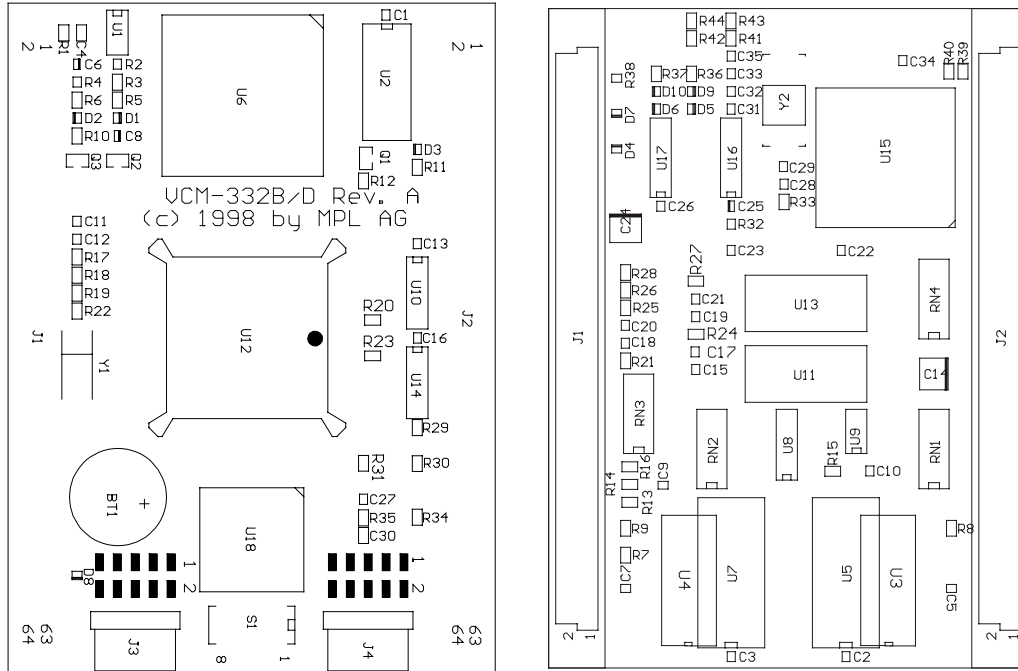
Processor:	Processor type:	MC68332
	Processor primary clock:	32.768KHz
	Processor speed:	VCM332B: DC to 16.78MHz (PLL) VCM332D: DC to 25.166MHz (PLL)
Memory:	Equipped:	256K byte or 1M byte SRAM, 256K byte or 1M byte FLASH 1024-bit serial EEPROM
	Not equipped:	Up to 512K byte 16-bit wide EPROM
Serial ports:	No. of ports	One TTL-level Two RS-232 level (without handshake)
		One 16-bit timer (68681)
Clock/timers:	Timers:	Various timers via 68332 TPU
		RTC72423, can be battery buffered
Connectors:	Clock/calendar:	One 10 pin (all three serial ports)
	Serial interface:	One 10 pin
	Debug interface:	Two 64 pin connectors
	I/O interface:	100% CMOS
Technology:	Surface mounted devices:	95.0 x 69 mm (3.75 x 2.75 in)
Mechanical specs:	Length x width:	15mm (0.6 in), including connector counterpart
	Overall height:	60 g (0.15 lb)
	Weight	0° to +70°C (+32° to +132°F)
Environment specs:	Temperature range:	-25° to +85°C (-13° to +185°F)
	Extended range:	20-90% non condensing
	Relative humidity:	+5V only / 140mA @ 16.78MHz
Power:	Power requirements:	4.75V to 5.25V
	Power range:	

Table 1.2 Technical characteristics

3. PREPARATION FOR USE

3.1 PARTS LOCATION

The diagram Fig. 2.1 shows the position of all components and connectors on the VCM332B/D.



3.1.1 CONNECTOR AND DIP SWITCH OVERVIEW

Name	Function
J1	Bus interface connector
J2	Peripheral signals and Bus interface connector
J3	Background debug 10 pin connector
J4	Serial interface 10 pin connector
S1	DIP switch configuration

Table 2.1.1 Switch and connector overview

3.2 TYPE AND SIZE OF MEMORY

3.2.1 SRAM

The on-board SRAM consists of two SMT-devices in byte organization. Their size is 128K byte x 8 (VCM332B/D-1) or 512K byte x 8 (VCM332B/D-2) which results in a total memory size of 256K byte or 1M byte. Device U5 (U3 for 25.166MHz zero Wait States operation) is connected to the lower data byte (D0 - D7), device U7 (U4 for 25.166MHz zero Wait States operation) to the upper data byte (D8 - D15). Both devices have independent chip-selects which allows for byte-by-byte accesses.

3.2.2 EPROM

The EPROM is not equipped. A socket is provided where 16-bit wide devices in 44 pin PLCC or JLCC package must be used. The following table lists the usable device-sizes and some manufacturers of these devices.

EPROM	Manufacturer	Device Nr.	Package type
1M bit	AMD	AM27C1024	PLCC44 / OTP
	Atmel	AT27C1024	PLCC44 / OTP
	Hitachi	HN27C1024	PLCC44 / OTP
		HN27C1024	JLCC44 / windowed
	Intel	27C220	PLCC44 / OTP
SGS	M27C1024	PLCC44 / OTP	
2M bit	AMD	AM27C2048	PLCC44 / OTP
	Atmel	AT27C2048	PLCC44 / OTP
4M bit	AMD	AM27C4096	PLCC44 / OTP
	Hitachi	HN27C4096	PLCC44 / OTP
		HN27C4096	JLCC44 / windowed
	SGS	M27C4002	PLCC44 / OTP
		M27C4002	JLCC44 / windowed
TI	TMS27PC240	PLCC44 / OTP	

Table 2.2.2 Type and size of EPROM

3.3 DIP SWITCH

3.3.1 DIP SWITCH CONFIGURATION (S1)

DIP switch S1 configures the board in accordance with the following table. The configuration will be set each time the board comes out of reset. The following paragraph contains a detailed description of the individual settings.

Switch No.	ON	OFF
1	CPU mode	SBC mode
2	4M bit SRAM	1M bit SRAM
3	4M bit EPROM	1 or 2M bit EPROM
4	DUART IRQ enabled	DUART IRQ disabled
5	Slave mode on	Slave mode off
6	Background mode on	Background mode off
7	Boot from EPROM	Boot from FLASH
8	SRAM/RTC battery buffered	Battery buffering off

Table 2.3.1 Configuration DIP switch

3.3.2 DIP SWITCH DESCRIPTION

Some of the MC68332's pins can perform a default or alternate function. Likewise internal modules can be switched on and off. Which pin or module function will be performed depends on the level of specific (data bus) pins when reset is released. However, each pin function can be redefined at run-time out of the application program.

Switch No. 1:

This switch selects two global modes. We call them "Single Board Computer (SBC)" or "Central Processing Unit (CPU)" mode.

When set to CPU mode, the MC68332 comes out of reset and is ready to perform like a real CPU: all address lines (A0 - A23), function code lines (FC0 - FC2), bus arbitration lines (BR, BG, BGACK) and all bus control signals are enabled. This mode is primarily intended for use of the VCM332B/D as master CPU in a bus system (e.g. G-64/96 bus).

The highest complexity is achieved if the VCM332B/D runs in SBC mode. After reset most pins of the MC68332 that alternately can perform a chip select function are configured so. This means, lines BR, BG, BGACK, A21 - A23 and FC0 - FC2 are defined as chip select outputs CS0 - CS5 and CS8 - CS10. Note that CS8 and CS9 are exclusively used by the SRAM and the DUART/RTC. On the VCM332D A20 is additionally configured as CS7 and exclusively used by the DUART (instead of sharing CS9 with the RTC).

Switch No. 2 and 3:

The SRAM and EPROM size has to be defined with these two switches. Since the SRAM is soldered directly to the PCB (in SMD), switch 2 is set by MPL AG. The position of the switch depends on the type of VCM332B/D (VCM332-1 or -2).

Switch No. 4:

The interrupt of DUART 68681 can be connected to IRQ-level 6 or be left unconnected. In this case, the DUART interrupt register has to be polled.

Switch No. 5:

In slave mode, the CPU32 of the 68332 is switched off. However, the internal peripherals can still be accessed via the external bus.

Switch No. 6:

In background debug mode, registers and memory can be viewed/alterd by special debugging hardware while the VCM332B/D is fully operational. This switch set to the OFF position prevents the VCM332 of falling into background debug mode when no debugging hardware is connected. This is important in normal applications where fatal errors (i.e. illegal instructions) would cause the MC68332 to fall in background debug mode and hence would let hang the system forever.

Switch No. 7

There are two possible boot memories, the EPROM and the FLASH. If set to OFF, the VCM332B/D boots from FLASH, otherwise it boots from EPROM.

NOTE

When booting from FLASH, an EPROM must not be equipped on the socket! Data corruption may result.

Switch No. 8

When ON, SRAM and RTC are battery buffered using the on-board battery or external battery (whichever has the greater output voltage).

For more information see also 4.2.1 MC68332 LOW LEVEL REGISTER INITIALISATION.

3.4 CONNECTORS

3.4.1 BUS INTERFACE CONNECTOR (J1)

The bus interface signals of the MC68332 are directly connected to 64-pin connector J1. Inputs and outputs with three-state capability have pull-up resistors (with exception of A0 - A20).

Signal names correspond to the denotation used in the 'MC68332 user's manual'. Signal description as well as signal type reflect the state after reset (e.g. Port E/F pin functions can be altered by software). The signal type as indicated in the column 'type' represents the view from the VCM332B/D.

Pin	Signal	Type	Note	Pin	Signal	Type	Note
1	GND			33	SIZ1	OUT	
2	+5V			34	FC0,CS3	OUT	(4)
3	+5V			35	FC1,CS4	OUT	(4)
4	+5V			36	FC2,CS5	OUT	(4)
5	VBat	IN	(1)	37	/DSACK0	IN	
6	VBat	IN	(1)	38	/DSACK1	IN	
7	VBB	OUT	(2)	39	/AVEC	IN	
8	/BERR	IN		40	A0	OUT	
9	D0	I/O		41	A8	OUT	
10	D1	I/O		42	A7	OUT	
11	D2	I/O		43	A6	OUT	
12	D3	I/O		44	A5	OUT	
13	D4	I/O		45	A4	OUT	
14	D5	I/O		46	A3	OUT	
15	D6	I/O		47	A2	OUT	
16	D7	I/O		48	A1	OUT	
17	D8	I/O		49	A16	OUT	
18	D9	I/O		50	A15	OUT	
19	D10	I/O		51	A14	OUT	
20	D11	I/O		52	A13	OUT	
21	D12	I/O		53	A12	OUT	
22	D13	I/O		54	A11	OUT	
23	D14	I/O		55	A10	OUT	
24	D15	I/O		56	A9	OUT	
25	/RES	OCO	(3)	57	A23,CS10	OUT	(4)
26	CLK OUT	OUT		58	A22,CS9	OUT	(4,5)
27	/HALT	OCI	(3)	59	A21,CS8	OUT	(4,5)
28	R/W	OUT		60	A20,CS7	OUT	(4,5,6)
29	/DS	OUT		61	A19	OUT	
30	/AS	OUT		62	A18	OUT	
31	/RMC	OUT		63	A17	OUT	
32	SIZ0	OUT		64	GND		

Table 2.4.1 Bus interface connector J1
Notes:

- (1) Pins 5 and 6 are wired together on the VCM332B/D. An external battery can be connected to these pins. Since there is already an on-board battery provided (7mAh capacity recharged with special circuit), the external battery can be used as an additional backup security for SRAM/RTC. A switch-over circuit automatically switches between on-board and external battery, dependent on higher output voltage. A battery undervoltage detector monitors the external battery voltage. To guarantee data retention, the battery voltage should be at least 2.3V. Total standby current of SRAM and RTC is typically 5 μ A (+25°C).
- (2) VBB is the output of the battery switch-over circuit. Therefore, it may be used for battery backup of additional devices. The maximum operating current of the devices connected to this pin should be limited to 150mA.
- (3) Reset is an active-low open drain output. Halt must be an active-low open drain input.
- (4) After reset, the function of these lines depends on the setting of dip switch 1 (CPU mode, SBC mode).
- (5) CS8 and CS9 (in SBC mode) cannot be used freely. They are exclusively used as chip selects for the internal SRAM and DUART/RTC.
- (6) CS7 (in SBC mode of VCM332D) cannot be used freely. It is used exclusively as chip select for the DUART while CS9 becomes an exclusive chip select for the RTC.

3.4.2 PERIPHERAL SIGNALS/ BUS INTERFACE CONNECTOR (J2)

Connector J2 contains the signals of the on-board peripherals as well as some bus control signals. Inputs and outputs with three-state capability have pull-up resistors (with exception of TP0 - TP15). The signals are directly connected to 64-pin connector J2, except the RS-232 lines which are converted and driven on-board. Signal names correspond to the denotation used in the '68332 user's manual' and the DUART 68681 data sheet.

IP0 - IP4 and OP0 - OP7 are the input/output ports of the DUART (IP5 is used internally). On pins 53 - 62, three serial ports with TTL- and/or RS232-level are available. RXD/TXD represent the 68332 SCI, RXDA/B and TXDA/B are the serial ports A and B of DUART 68681.

Signal description as well as signal type reflect the state after reset (e.g. Port E/F pin functions can be altered by software). The signal type as indicated in the column 'type' represents the view from the VCM332B/D.

Pin	Signl	Type	Note	Pin	Signl	Type	Note
1	GND			33	TP10	I/O	(7)
2	/CSBoot	OUT	(1)	34	TP11	I/O	(7)
3	RES	OUT	(2)	35	TP12	I/O	(7)
4	RES-SW	IN	(3)	36	TP13	I/O	(7)
5	/BR,CS0	I/O	(4)	37	TP14	I/O	(7)
6	/BG,CS1	OUT	(4)	38	TP15	I/O	(7)
7	/BGACK, CS2	I/O	(4)	39	T2CLK	IN	
8	MISO	I/O		40	IP0	IN	
9	MOSI	I/O		41	IP1	IN	
10	SCK	I/O		42	IP2	IN	
11	/PCS0,SS	I/O		43	IP3	IN	
12	/PCS1	OUT		44	IP4	IN	
13	/PCS2	OUT		45	OP0	OUT	
14	/TSTME	IN		46	OP1	OUT	
15	MODC	IN	(5)	47	OP2	OUT	
16	/IRQ1	IN		48	OP3	OUT	
17	/IRQ2	IN		49	OP4	OUT	
18	/IRQ3	IN		50	OP5	OUT	
19	/IRQ4	IN		51	OP6	OUT	
20	/IRQ5	IN		52	OP7	OUT	
21	/IRQ6	OCI	(6)	53	TXD	RS232	
22	/IRQ7	IN		54	RXD	RS232	(8)
23	TP0	I/O	(7)	55	TXDB	RS232	
24	TP1	I/O	(7)	56	RXDB	RS232	(8)
25	TP2	I/O	(7)	57	TXDA	TTL	
26	TP3	I/O	(7)	58	RXDA	TTL	
27	TP4	I/O	(7)	59	TXDB	TTL	
28	TP5	I/O	(7)	60	RXDB	TTL	(8)
29	TP6	I/O	(7)	61	RXD	TTL	(8)
30	TP7	I/O	(7)	62	TXD	TTL	
31	TP8	I/O	(7)	63	GND		
32	TP9	I/O	(7)	64	GND		

Table 2.4.2 Connector J2

Notes:

- (1) CSBoot is used as chip select for the internal EPROM (or FLASH if S1/1 is switched OFF).
- (2) Reset is an active-high output.
- (3) A reset-switch (to GND) can be connected to this pin. A pull-up resistor is provided on-board. A closure on this switch resets the VCM332B/D.
- (4) After reset, the function of these lines depends on the setting of dip switch 1 (CPU mode,SBC mode).
- (5) MODC has an internal pull-up resistor. Therefore, after reset the software watchdog is not prescaled.
- (6) IRQ6 is the only interrupt used by the VCM332B/D (DUART 68681 interrupt). If desired, it can be switched off with dip switch 4.
- (7) After reset, TPU lines TP0 - TP15 are inputs and do not have pull-up or pull-down resistors. To prevent a floating state, they have to be leveled externally.
- (8) Inputs RxD/pin 61 and RxD/pin 54 (after back-transformation to TTL level) are internally connected together. Don't use them in parallel, leave one input open! Connecting both inputs would not damage the drivers (on-board short circuit protection), but corrupt the received data. The above is true for RxD/pin 60 and RxD/pin 56 as well.

3.4.3 BACKGROUND DEBUG CONNECTOR (J3)

Connector J3 offers an interface to interconnect the on-chip 68332 background debug monitor to external debug hard- and software. Signal names correspond to the denotation used in the '68332 user's manual'. The connector pin-out is compatible to Motorola's definition.

Pin	Signal	Description
1	/DS	Data strobe
2	/BERR	Bus error
3	GND	Ground
4	/BKPT, DSCLK	Signals a hardware breakpoint to the MC68332 / serial clock in background debug mode
5	GND	Ground
6	FREEZE	Indicates that the CPU has acknowledged a breakpoint
7	/RES	Indicates a reset to/from the VCM332B/D
8	/IFETCH, DSI	Indicates an instruction word fetch / serial input data in background debug mode
9	VCC	+5V power
10	/IPIPE, DSO	Used to track movement of words through the instruction pipeline / serial output data in background debug mode

Table 2.4.3 Background debug connector J3

For more information about the Background debug interface see also 3.3.2.3 BACKGROUND DEBUG INTERFACE

3.4.4 SERIAL INTERFACE CONNECTOR (J4)

J4 allows the connection of two serial RS-232 ports (without handshake) and one serial TTL port (with handshake). All RS-232 output signals have a typical voltage range of ± 9 Volts. Signal names correspond to the denotation used in the '68332 user's manual' and the DUART 68681 data sheet.

Pin	Signal	Description
1	TXDB	TXD port B 68681 (RS232 level)
2	RXDB	RXD port B 68681 (RS232 level)
3	TXD	TXD SCI 68332 (RS232 level)
4	RXD	RXD SCI 68332 (RS232 level)
5	GND	Ground
6	TXDA	TXD port A 68681 (TTL level)
7	RXDA	RXD port A 68681 (TTL level)
8	OP0	RTS port A 68681 or free output (TTL level)
9	IP0	CTS port A 68681 or free input (TTL level)
10	VCC	+5V power

Table 2.4.4 Serial interface connector J4

Note

The serial ports are also available on bus interface connector J2. Don't use them in parallel!

4. OPERATION

4.1 MEMORY MAP

The VCM332B/D offers two different memory maps, dependant on the setting of dip switch 1. However, the memory maps differ only slightly as detailed below.

4.1.1 SBC MEMORY MAP

Address space	Space name	16-bit port even (D15-D8)	16-bit port odd (D7-D0)	Note
FFFFFF				
FFF000	68332 reg.			
FFEFFF				
300000	Not used			(1)
2FFFFFF				
200000	FLASH	X	X	(2)
1FFFFFF				
100000	SRAM	X (U7/U4)	X (U5/U3)	
0FFFFFF				
0E0000	RTC		X	(3)
0DFFFF				
0C0000	DUART		X	
07FFFF				
000000	EPROM/FLASH	X	X	(4)

Table 3.1.1 SBC memory map

Notes:

- (1) Intended for use with an expansion board. Accesses to this memory space have to be programmed via the 68332 chip-select submodule (only address lines A0 - A20 on VCM332B or A0-A19 on VCM332D respectively are available).
- (2) Only valid if S1/7 is switched to ON.
- (3) Only the lower 4 bits are used (D3 - D0).
- (4) EPROM is the boot memory if S1/7 is switched to ON, otherwise the FLASH acts as boot memory.

4.1.2 CPU MEMORY MAP

Address space	Space name	16-bit port even (D15-D8)	16-bit port odd (D7-D0)	Note
FFFFFF				
FFF000	68332 reg.			
FF0000	free			
E00000				
300000	VMA	X	X	(1)
200000	FLASH	X	X	(2)
100000	SRAM	X (U7/U4)	X (U5/U3)	
000000				
0E0000	RTC		X	(3)
000000				
0C0000	DUART		X	
0B0000				
0A0000	VPA async.	X	X	(1)
090000				
080000	VPA sync.	X	X	(1)
070000				
000000	EPROM/FLASH	X	X	(4)

Table 3.1.2 CPU memory map

Notes:

- (1) The VPA/VMA space is used in a G-96 bus environment for decoding of peripheral/memory bus devices. The spaces are adjusted to the G-96 EPLD from MPL AG. If not used this particular way, the memory space is free for use and can be decoded using address lines A0 - A23.
- (2) Only valid if S1/7 is switched to ON.
- (3) Only the lower 4 bits are used (D3 - D0).
- (4) EPROM is the boot memory if S1/7 is switched to ON, otherwise the FLASH acts as boot memory.

4.1.3 MC68332 INTERNAL MODULE MEMORY MAP

Address	Internal module
YFFFFFF	
YFFE00	Time Processing Unit
YFFDFF	
YFFC00	Queued Serial Module
YFFB3F	
YFFB00	RAM Control
YFFA7F	
YFFA00	System Integration Module
YFF800	
YFF000	RAM array

Table 3.1.3 Internal module memory map

Where 'Y' stands for '7' or 'F' depending on the mod map bit setting in the module configuration register.

4.1.4 MC68332 CHIP SELECT USAGE

There are a few restrictions when using CS outputs on the VCM332B/D. For achieving minimum board size, the SRAM and peripherals on the VCM332B/D use chip select generators of the MC68332. They are used internally (of the MC68332) when running in CPU mode or externally (corresponding pins of the MC68332 are acting as chip select outputs) when running in SBC mode. The following table shows how they are used.

PIN	VCM332B		VCM332D	
	EXTERNAL	INTERNAL	EXTERNAL	INTERNAL
CS5/A18	A18	AVEC DUART	A18	AVEC DUART
CS6/A19	A19	not used	A19	Not used
CS7/A20	A20	not used	CS7(DUART)	External DSACK DUART
CS8/A21	CS8(RAM)	DSACK RAM	CS8(RAM)	DSACK RAM
CS9/A22	CS9(RTC/DUART)	DSACK RTC/DUART	CS9(RTC)	DSACK RTC
CS10/A23/E	CS10(FLASH)	DSACK FLASH	CS10(FLASH)	DSACK FLASH

Table 3.1.4A Chip select usage SBC mode

PIN	VCM332B		VCM332D	
	EXTERNAL	INTERNAL	EXTERNAL	INTERNAL
CS5/A18	A18	AVEC DUART	A18	AVEC DUART
CS6/A19	A19	DSACK RAM-L 16bit	A19	DSACK RAM-L 16bit
CS7/A20	A20	not used	A20	External DSACK DUART
CS8/A21	A21	DSACK RAM-H 16bit	A21	DSACK RAM-H 16bit
CS9/A22T	A22	DSACK RTC/DUART	A22	DSACK RTC
CS10/A23/E	A23	DSACK FLASH	A23	DSACK FLASH

Table 3.1.4B Chip select usage CPU mode

Signals A19, A20/CS7, A21/CS8 and A22/CS9 are always used and must be initialised as described in MC68332 LOW LEVEL REGISTER INITIALISATION. All other chip selects, except those described above, can be used freely and assigned for chip select outputs when running in SBC mode. In CPU mode, all addresses must be available externally to get the whole address range for external decoding.

4.2 DEVICE DESCRIPTION

4.2.1 MC68332 LOW LEVEL REGISTER INITIALISATION

4.2.1.1 INTRODUCTION INTO MC68332 INITIALISATION

Before the board is ready to work the internal registers of the MC68332 have to be initialised. The following paragraphs describe how and why the registers should be set up. Note that base addresses given in the examples correspond with the memory map and must not be changed in software. If a special memory map is desired please consult MPL AG or your local distributor.

For a more detailed description of the MC68332 see also the MC68332 manual available from your local Motorola distributor or as a downloadable pdf-file on the Motorola Web page (www.mot.com).

To allow for a sophisticated setting of the wait state count of the different memories and peripherals the following paragraphs give exact equations to calculate them. This may help the user to determine the exact processor clock frequency to run his application at maximum speed.

Sometimes the system runs faster with a slightly slower clock if one wait state can be saved compared to the faster clock. This effect is highly application specific. It depends on how much CPU time is required for the different function blocks on the VCM332B/D and on the connected application specific peripherals and how the wait state count of these function blocks decreases in relation to the slower clock.

4.2.1.2 CLOCK SYNTHESIZER

The MC68332 has a 32.768KHz crystal on its clock input. This results in a default clock speed of 8.38MHz following reset. This frequency can be changed by programming the SYNCR (Clock Synthesiser Control Register). The following example shows how to program the SYNCR for maximum clock frequency. Note that the VCM332B is designed to work from DC up to 16.777MHz while the VCM332D is capable to run up to 25.166MHz.

set SYNCR to \$CF08
set SYNCR to \$AF08

clock=16.777MHz, rest default (setting for VCM332B)
clock=25.166MHz, rest default (setting for VCM332D)

NOTE

Any clock set greater than stated above is not supported and may not work correctly with the VCM332B/D.

4.2.1.3 WATCHDOG

The watchdog is an on-chip function of the MC68332 which helps to recover after a fatal software error. For example a never ending loop will be terminated after the watchdog times out. If the software watchdog is enabled a special sequence has to be executed on a periodic basis. If the software running on the VCM332B/D doesn't use or service the SWSR the watchdog has to be disabled in the first few instructions after reset. This must be done so early because the watchdog is enabled after resetting the MC68332. All watchdog related bits reside in the SYPCR (System Protection Control Register) and in the SWSR (Software Service Register).

SYPCR set to %0000xxxx disable watchdog, rest as programmed

NOTE

The SYPCR can only be written once! Besides the watchdog configuration, the setup bits for the halt monitor and the bus error logic reside in this register.

4.2.1.4 BUS ERROR LOGIC

The VCM332B/D board has no bus error logic apart from that in the MC68332. This means that only bus transfers initiated by the MC68332 are monitored and, if necessary after the programmed time-out period aborted with a bus error. The bus monitor is following a reset programmed only for MC68332 internal devices. If external bus monitoring is desired the corresponding bits in the SYPCR have to be set correctly. If the bus monitor is disabled any access to an area where there is no DSACK source, will end in an indefinite long access to that location. If this occurs the processor must be reset. All bus error logic related bits are in the SYPCR.

SYPCR set to %xxxxxx101 enable bus monitor with 32 sysclock timeout,
this is recommended for 16.777MHz operation

SYPCR set to %xxxxxx100 enable bus monitor with 64 sysclock timeout,
this is recommended for 25.166MHz operation

NOTE

The SYPCR can only be written once! Besides the bus error logic configuration, the setup bits for the halt monitor and the watchdog reside in this register.

4.2.1.5 INITIALISATION OF MC68332 INTERNAL CHIP SELECT GENERATORS

Each chip select is set up by two registers, independent whether used only internally by the MC68332 or routed to the corresponding pin of the processor. These registers are

- 1) The CSORx: Chip Select Option Register
- 2) And the CSBARx: Chip Select Base Address Register.

Where x stands for the chip select numbers 0 to 10 respectively BT for the boot chip select.

A detailed description of these registers can be found in the MC68332 manual from Motorola. This paragraph gives a short description of these registers, while following chapters detail the chip select setup related to the VCM332 modules.

The CSBARx contains the information of starting address and size of the corresponding memory block. Bits 15 to 3 dictate the starting address where Bit 15 corresponds to address line A23, bit 14 to A22 down on to bit 3 which corresponds to A11. The block size is encoded by bits 2 to 0. In ascending order the binary values of this bit field with bit 2 as MSB correspond to block sizes of 2k, 8k, 16k, 64k, 128k, 256k, 512k and 1MByte. It is strongly recommended to use the memory mapping proposed in this manual and to set memory block sizes as close as possible to the physical memory on board the VCM332.

A more complex functionality is assigned to the CSORx. It is not within the scope of this manual to explain every bit setting in this register, please refer the MC68332 manual for the details. The following paragraphs give recommendations for CSORx setup. The bit positions marked with 'w' are standing for the binary encoded wait state count. A maximum of 13 wait states is adjustable.

4.2.1.5.1 SRAM CHIP SELECT GENERATOR

The VCM332B/D contains two SRAM memory chips. These chips can be either 128KByte or 512KByte which results in 256KByte or 1MByte of SRAM always linear accessible from a base address upwards to higher memory.

The VCM332-module takes advantage of the MC68332 internal chip select generator. To properly set up this machine it is necessary to distinguish between the two operating modes of the VCM332.

In the CPU mode (S1/1 set to the ON position) two internal chip select generators must be dedicated for generating DSACK's. One is responsible for the high byte and the other one for the low byte. The reason for this is because of the Pin Assignment Register Bit Encoding. If a chip select is internally used and the corresponding output is used as the default function, then the port size is automatically set to 16bit. In the CPU mode it isn't important which unused DSACK generators are used for that task but the initialisation should be made as described later.

In the SBC mode however chip select 8 is dedicated in 16 bit mode to handle both the high and the low byte.

Following the proposed register setting for the SRAM chip select registers:

In CPU mode

CSBAR6	set to	%0001 0000 0000 0 $_{SSS}$	where $_{SSS}$ stands for block size encoding
CSBAR8	set to	%0001 0000 0000 0 $_{SSS}$	where $_{SSS}$ stands for block size encoding
CSOR6	set to	%0011 10 $_{ww}$ $_{ww}11$ 0000	where $_{www}$ stands for wait state count
CSOR8	set to	%0101 10 $_{ww}$ $_{ww}11$ 0000	where $_{www}$ stands for wait state count

In SBC mode

CSBAR8	set to	%0001 0000 0000 0 $_{SSS}$	where $_{SSS}$ stands for block size encoding
CSOR8	set to	%0111 10 $_{ww}$ $_{ww}11$ 0000	where $_{www}$ stands for wait state count

4.2.1.5.1.1 SRAM WAIT STATE CALCULATION

For maximum performance when accessing the SRAM's the minimum wait state count needed at certain system clock frequencies can be derived out of the following equation:

$$WS \geq ((t_{V_{CMS}} + t_{SRAM}) / t_{CLK}) - 2$$

Where:

WS	Wait state count
$t_{V_{CMS}}$	A variant dependent constant that is 60ns for the VCM332D and 70ns for the VCM332B
t_{SRAM}	Access time of the SRAM chips
t_{CLK}	Processor clock period

NOTE

From on Rev. A of the VCM332B/D (MEL-10073-001), which is covered by this manual, MPL AG guarantees to equip VCM332B-boards with SRAM's of speeds of 70ns or faster. VCM332D-boards are equipped with parts of speeds of 50ns or faster. On request there may be VCM332D variants equipped with SRAM's of 20ns or faster speed grades. In this case a zero wait state operation at 25MHz is possible but SRAM's can't any longer be battery backed due to the high current consumption of these parts.

With this equipment, standard variants of the VCM332 can be run with 1 wait state at full speed.

4.2.1.5.2 EPROM CHIP SELECT GENERATOR

The EPROM mounted on the VCM332B/D is directly connected to the CSBOOT output of the MC68332. The CSBOOT is dedicated to access the boot memory and is valid and activated after reset.

The default value of the CSBARBT (Chip Select Base Address Register Boot) after reset adjusts for a base address of \$00000000 and a memory block size of 1Mbyte. Because the maximum amount of EPROM on the VCM332B/D is 512Kbyte this register has to be changed to a maximum block size of 512Kbyte or the size the currently used EPROM has.

The CSORBT (Chip Select Option Register Boot) is set to 13 wait states as its default after reset. It is not absolutely necessary to change this value but for faster program operation it is strongly recommended to set the value according the equation of paragraph 4.2.1.5.2.1 EPROM WAIT STATE CALCULATION.

Following the proposed register setting for the EPROM boot chip select registers (not necessarily to be modified):

In CPU and SBC mode

CSBARBT set to %0000 0000 0000 0_{sss} where sss stands for block size encoding

CSORBT set to %0110 10_{ww} ww00 0000 where ww stands for wait state count

4.2.1.5.2.1 EPROM WAIT STATE CALCULATION

For maximum performance when accessing the EPROM the minimum wait state count needed at certain system clock frequencies can be derived out of the following equation:

$$WS \geq ((t_{VCME} + t_{ROM}) / t_{CLK}) - 2$$

Where:

WS Wait state count

t_{VCME} A variant dependent constant that is 30ns for the VCM332D and 40ns for the VCM332B

t_{ROM} Access time of the EPROM chip

t_{CLK} Processor clock period

NOTE

The EPROM can exclusively be used as boot memory. If the VCM332 is to be booted from FLASH (S1/7 switched OFF) no EPROM must be inserted in socket U6.

4.2.1.5.3 FLASH CHIP SELECT GENERATOR

This chapter discusses the correct wait state calculation and CSOR setup for the FLASH memories. A more detailed view of the FLASH itself is provided in chapter 5.1 ACCESSING ON BOARD FLASH.

The VCM332B/D can be equipped with FLASH memory sizes of 256KByte, 512KByte or 1MByte. In all cases the entire memory is realised with two 8 bit wide chips. However they form a 16 bit wide port to the processor and must always be programmed in parallel.

Following the proposed register setting for the FLASH chip select registers. If used as boot memory, setup of chip select boot registers is similar to the EPROM setup.

In CPU and SBC mode

CSBAR10 set to %0010 0000 0000 0_{sss} where sss stands for block size encoding

CSOR10 set to %0111 10_{ww} ww11 0000 where ww stands for wait state count

Since the FLASH can be used as either boot memory or conventional non volatile memory there has to be distinguished between these two cases for wait state calculation.

4.2.1.5.3.1 WAIT STATE CALCULATION FOR FLASH AS NON VOLATILE MEMORY

As non volatile memory the FLASH resides at base address \$200000. CS10 is dedicated for the FLASH in SBC mode and recommended for use in CPU mode. The correct number of wait states can be derived out of the following equation:

$$WS \geq ((t_{VCMFN} + t_{FLASH}) / t_{CLK}) - 2$$

Where:

WS Wait state count

T_{VCMFN} A variant dependent constant that is 70ns for the VCM332D and 80ns for the VCM332B

t_{FLASH} Access time of the FLASH chips

t_{CLK} Processor clock period

NOTE

From on Rev. A of the VCM332B/D (MEL-10073-001), which is covered by this manual, MPL AG guarantees to equip VCM332B-boards with FLASH's of speeds of 150ns or faster. VCM332D-boards are equipped with parts of speeds of 100ns or faster.

This results in wait state counts of 2 for VCM332B and 3 for VCM332D each at full speed.

4.2.1.5.3.2 WAIT STATE CALCULATION FOR FLASH AS BOOT MEMORY

By switching S1/7 to the OFF position the FLASH becomes the boot memory. Care must be taken that now CSBOOT has to be set up to access the FLASH. Due to the different hardware implementation of CSBOOT compared to CS10 the wait state calculation slightly differs:

$$WS \geq ((t_{VCMFB} + t_{FLASH}) / t_{CLK}) - 2$$

Where:

WS Wait state count

T_{VCMFB} A variant dependent constant that is 30ns for the VCM332D and 40ns for the VCM332B

t_{FLASH} Access time of the FLASH chips

t_{CLK} Processor clock period

NOTE

From on Rev. A of the VCM332B/D (MEL-10073-001), which is covered by this manual, MPL AG guarantees to equip VCM332B-boards with FLASH's of speeds of 150ns or faster. VCM332D-boards are equipped with parts of speeds of 100ns or faster.

This results in a wait state count of 2 at full speed, independent of the variant.

4.2.1.5.4 EXTERNAL PERIPHERY CHIP SELECT GENERATOR

The VCM332B/D contains a real time clock RTC72423 and a serial interface chip MC68681. The main difference between hardware implementations of the VCM332B and the VCM332D is in the way the external periphery is connected to the MC68332. While on the VCM332B both external chips are handled by a single chip select, they had to be split to two chip selects on the VCM332D. However in common to both variants is that the 8 bit wide chips are connected like they were 16 bits wide. Due to this, the individual registers of these chips are only accessible on odd bytes. The even byte lane is not connected! In addition the RTC only requires the lower 4 bits of the odd byte. The reason for this connection scheme is software compatibility to existing G-64/96 environments.

4.2.1.5.4.1 VCM332B PERIPHERY CHIP SELECT

On the VCM332B for both (the RTC and the DUART) chip select 9 is dedicated in SBC mode. It is recommended, that in CPU mode the same chip select is used to generate the DSACK internally. CS9 (in SBC mode) in conjunction with address line A17 form the individual chip selects for the two peripherals. In CPU mode the chip selects are hard decoded from address lines A17 to A23.

If the MC68681 uses interrupts an AVEC generator is also needed. This is established by setting up an additional chip select to create the AVEC response to the MC68332. Please refer chapter 4.2.1.5.5 DUART AVEC GENERATOR for further information.

Following the proposed register setting for the periphery chip select registers:

In CPU and SBC mode

CSBAR9 set to %0000 1100 0000 0101

CSOR9 set to %0111 10ww ww11 0000 where www stands for wait state count

4.2.1.5.4.1.1 WAIT STATE CALCULATION FOR VCM332B PERIPHERY

Since the DUART MC68681 is the slower of the two devices it is sufficient if the wait state calculation refers only to the timing of this chip. Following equation must be fulfilled to satisfy its need:

$$WS \geq (790ns / t_{CLK}) - 2$$

Where:

WS Wait state count

t_{CLK} Processor clock period

4.2.1.5.4.2 VCM332D PERIPHERY CHIP SELECT

In addition to chip select 9, which is exclusively dedicated to the RTC, chip select 7 is routed to the DUART in SBC mode. It is recommended, that in CPU mode the same chip selects are to be used internally. Both chip selects form in conjunction with address line A17 the individual chip selects for the assigned peripherals in SBC mode. In CPU mode the chip selects are hard decoded from address lines A17 to A23.

If the MC68681 uses interrupts an AVEC generator is also needed. This is established by setting up an additional chip select to create the AVEC response to the MC68332. Please refer to chapter 4.2.1.5.5 DUART AVEC GENERATOR for further information.

Following the proposed register setting for the periphery chip select registers:

In CPU and SBC mode

CSBAR7	set to	%0000	1100	0000	0000	
CSBAR9	set to	%0000	1110	0000	0000	
CSOR7	set to	%0111	1011	1111	0000	
CSOR9	set to	%0111	10 _{ww}	ww11	0000	where www stands for wait state count

4.2.1.5.4.2.1 WAIT STATE CALCULATION FOR VCM332D RTC

Compared to the VCM332B, on the VCM332D the RTC is the only device residing on CS9 in SBC mode. Thus it are its timing requirements dictating the wait state count for CS9:

$$WS \geq (215ns / t_{CLK}) - 2$$

Where:

WS	Wait state count
t _{CLK}	Processor clock period

4.2.1.5.4.2.2 WAIT STATE CALCULATION FOR VCM332D DUART

Since the DUART operates off an own clock generator the worst case access times may could exceed the access time that can be generated internally the MC68332 operating at 25MHz. This is the reason for separating the DUART chip select from the RTC chip select on the VCM332D. It now operates asynchronously and generates the DSACK externally. So the CSOR register has to be set to external DSACK and no wait state calculation is needed.

4.2.1.5.5 DUART AVEC GENERATOR

When the DUART interrupt is enabled with dip switch position 4, the MC68332 has to make an internal AVEC generator available which generates an internal AVEC signal in the case a DUART interrupt occurs.

The DUART interrupt is hardwired via dip switch 4 with IRQ6 of the MC68332. The DUART interrupt can only be used in the auto vectored mode. The initialisation example shows how to set up a chip select option register to work as an AVEC generator. There is no restriction which chip select register is used because the AVEC signal is only used internally by the MC68332.

Following the proposed register setting for the autovector chip select registers:

In CPU and SBC mode

CSBAR5	set to	%1111	1111	1111	1000
CSOR5	set to	%0010	1000	0000	1101

4.2.1.6 EXAMPLE OF REGISTER INITIALISATION

This initialisation example shows a possible setup for the chip select generators. The different variants of the board are covered with conditional assembly directives. To reduce complexity a VCM332 with 512 kByte SRAM, 1 MByte FLASH and a 512 kByte EPROM is assumed. Real life initialisation may be held simpler (if only one hardware variant has to be supported) or becomes more complex (when supporting all possible hardware variants and additional customer specific circuits).

** first of all disable Watchdog, set bus monitor timeout*

** and set system clock according the variant*

```
ifdef VCM332B
    move.b #05,$ffa21 ; SYPCR: set to watchdog off and 32 sysclock bus timeout at 16MHz
    move.w #cf08,$ffa04 ; SYNCR: setup full speed clok of 16.78 MHz for VCM332B
else
    ; is VCM332D
    move.b #04,$ffa21 ; SYPCR: set to watchdog off and 64 sysclock bus timeout at 25MHz
    move.w #saf08,$ffa04 ; SYNCR: setup full speed clok of 25.17 MHz for VCM332D
endc
```

** setup of the SRAM depends on the operating mode*

```
    move.w #1006,$ffa64 ; CSBAR6: baseaddress = $10 0000 and blocksize=512K common to all modes
    move.w #1006,$ffa6c ; CSBAR8: baseaddress = $10 0000 and blocksize=512K common to all modes
ifdef SBC
    move.w #03F5,$ffa46 ; CSPAR1 doesn't really need to be set since it will be set during reset
    move.w #7870,$ffa6e ; CSOR8: handle both bytes in SBC mode with 1 wait state
else
    ; is in CPU mode
    move.w #0155,$ffa46 ; CSPAR1 doesn't really need to be set since it will be set during reset
    move.w #3870,$ffa66 ; CSOR6: handle lower byte in CPU mode with 1 wait state
    move.w #5870,$ffa6e ; CSOR8: handle upper byte in CPU mode with 1 wait state
endc
```

** setup of the EPROM is dependent on its speed (assumed 120ns) and on the VCM variant*

```
    move.w #0006,$ffa48 ; CSBARBT: baseaddress=0 and blocksize=512K
ifdef VCM332B
    move.w #7870,$ffa4a ; CSORBT: handle both bytes with 1 WS
else
    ; is VCM332D
    move.w #78b0,$ffa4a ; CSORBT: handle both bytes with 2 WS
endc
```

** setup of the FLASH is dependent on the VCM variant*

```
    move.w #2007,$ffa74 ; CSBAR10: baseaddress=$20 0000 and blocksize=1M
ifdef VCM332B
    move.w #78b0,$ffa76 ; CSOR10: handle both bytes with 2 WS
else
    ; is VCM332D
    move.w #78f0,$ffa76 ; CSOR10: handle both bytes with 3 WS
endc
```

** setup of the Peripherals is dependent on the variant*

```
ifdef VCM332B
    move.w #0c05,$ffa70 ; CSBAR9: baseaddress=$0c 0000 and blocksize=256K
    move.w #7b30,$ffa72 ; CSOR9: handle both bytes with 12 WS
else
    ; is VCM332D
    move.w #0c00,$ffa68 ; CSBAR7: baseaddress=$0c 0000 and blocksize=2K
    move.w #0e00,$ffa70 ; CSBAR9: baseaddress=$0e 0000 and blocksize=2K
    move.w #7bf0,$ffa6a ; CSOR7: handle both bytes with external DSACK
    move.w #7930,$ffa72 ; CSOR9: handle both bytes with 4 WS
endc
```

** setup of AVEC response for INT6 is independent of the variant*

```
    move.w #FFF8,$ffa60 ; CSBAR5
    move.w #280D,$ffa62 ; CSOR5: set for autovector response
```

4.2.2 MC68332 INTERNAL PERIPHERALS

4.2.2.1 TIME PROCESSING UNIT

The Time Processing Unit (TPU) performs both simple and complex timing tasks. All TPU input and/or output pins are directly (not filtered nor ESD protected) available on J2. Out of reset the TPU lines are defined as inputs and are floating on board the VCM332. For this reason it is necessary to pull up or down these lines on the motherboard to prevent malfunction of the MC68332.

For a more detailed description please consult the TPU manual.

4.2.2.2 QUEUED SERIAL MODULE

The QSM (Queued Serial Module) provides the microprocessor with two serial communication interfaces divided into two sub modules: the (QSPI) Queued Serial Peripheral Interface and the SCI (Serial Communications interface). The QSPI is a full duplex, synchronous serial interface for communication with peripherals and other MCUs. It is enhanced by the addition of a queue for receive and transmit data. It's signals are all available on J2. The SCI is a full duplex universal asynchronous receiver / transmitter (UART) serial interface. These sub-modules operate independently. The SCI's input and output pins are available on J2 as well as on J4.

For a more detailed description please consult the QSM manual.

4.2.2.3 BACKGROUND DEBUG INTERFACE

The BDM (Background Debug Mode) available through the 10 pin connector J3 is a special debugger which is directly implemented in micro code in the MC68332 processor. This debugger allows reading and/or changing of a register or memory as well as invoking test features. The BDM is enabled after reset when dip switch 6 is ON.

The background debug connector holds all relevant signals used for the ABATRON debug interface or for the BD32 (Background mode Debugger for the MC68332) which is available from Motorola.

With the type of tools mentioned above the software engineer is capable of downloading programs or test software without ever burning an EPROM.

4.2.2.4 CHIP SELECT MODULE

When using the VCM332B/D in the CPU mode as well as in the SBC mode, specific chip selects must be used as described in 4.2.1.5 INITIALISATION OF MC68332 INTERNAL CHIP SELECT GENERATORS. The remaining chip selects can be used for application specific purposes. Please refer the MC68332 manual for details to chip select and pin assignment registers. Please note, that the pin assignment registers (CSPAR0 and CSPAR1) don't need to be changed if the VCM332 is used "stand alone". They will be set up for proper operation in either (CPU and SBC) mode during setup.

4.2.2.5 PORT E AND PORT F PIN ASSIGNMENT

Port E holds either a general purpose input/output port or bus control signals like SIZ0, SIZ1,, DSACK0, DSACK1. The signals that the VCM332B/D uses as bus controls are DS*, AS*, SIZ0 and, for the VCM332D, DSACK1. The others can be used as general purpose I/O's.

Port F holds either the general purpose I/O port F, or all interrupt inputs as well as the MODCK select input. The VCM332B/D only makes use of IRQ6 for the DUART interrupt. It is recommended to reserve this input for IRQ6 even if the DUART interrupt is disabled by S1/4. All others can be freely used as general purpose I/O ports or interrupt inputs.

All of the port E and port F pins are on board the VCM332 leveled, so that no external pull up or pull down resistors are needed.

4.2.3 RTC 72423 REAL TIME CLOCK

The real time clock is the RTC72423 from SEIKO. The circuit is clocked with an integrated 32.768KHz crystal oscillator and offers date and time functions. For more information see the data sheet RTC72423 from SEIKO.

Note

The STD.P output of the RTC72423 is not used.

4.2.4 KS93C46 SERIAL EEPROM

The equipped serial EEPROM is a 1024bit memory device, organised in 64 registers of 16bits each. It can be programmed, read or written via the MC68332's SPI interface set up as a master on the SPI. The phase and polarity should be programmed in the following way in the SPCR0 (QSPI Control Register 0).

SPCR0(CPHA) set to 1
SPCR0(CPOL) set to 1

The following figure shows the interconnection between the EEPROM and the SPI interface.

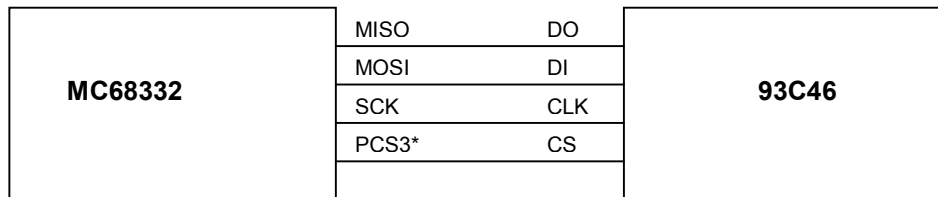


Fig. 3.2.4.: Interconnection MC68332 – EEPROM

NOTE

Comparing EEPROM devices with the part number '93C46' shows differences in the programming sequence: Some devices do not need erase and/or erase all instruction prior to a write and/or write all instruction since they erase automatically on write/write all instructions. MPL can not guarantee to generally equip the VCM332B/D with devices with or without automatic erase feature. Therefore, the 3-wire serial EEPROMs equipped on the VCM332B/D require an erase and erase all cycle prior to a write and write all instruction! Some of the manufacturers listed below offer devices with automatic erase feature. However, they all have to be programmed in the conservative way. The following data sheets should be consulted: Samsung (KM93C46), Hyundai (HY93C46), SGS-Thomson (ST93C46A), Catalyst Semiconductor (CAT93C46), OKI (MSM16811RS), Atmel (AT93C46), National Semiconductor (NMC93C46).

4.2.5 MC68681 DUART AND GENERAL PURPOSE I/O

The Dual Universal Asynchronous Receiver and Transmitter (DUART) 68C681 (XR68C681, SCC68692) is used for the serial interface. It consists of two serial channels with independently programmable baud rates from 50 to 38400 baud. Each channel can be used as a 5-wire communication interface (TXD, RXD, RTS, CTS and GND). The 68C681 also contains a 16bit counter/timer which can be used separately or as a baud rate generator creating special baud rates. Vectored interrupts from the 68C681 are not supported by the VCM332B/D. The interrupt of the 68C681 is treated as auto vectored on request level 6. The interrupt can be disabled by the help of configuration dip switch 4. The DUART is clocked with a 3.6864MHz crystal oscillator. Besides these features there is an 8bit output port and a 6bit input port which can be partly used as multipurpose I/Os. Some of these port bits are used for the serial communication, and one has a special function within the VCM332B/D. Both ports are described below.

IP0	CTS channel A or multipurpose input
IP1	CTS channel B or multipurpose input
IP2	multipurpose input
IP3	multipurpose input
IP4	multipurpose input
IP5	Battery indicator '1' battery is ok , '0' battery voltage dropped below 2.2V
IP6	no function
IP7	no function
OP0	RTS channel A or multipurpose output
OP1	RTS channel B or multipurpose output
OP2	multipurpose output
OP3	multipurpose output
OP4	multipurpose output
OP5	multipurpose output
OP6	multipurpose output
OP7	multipurpose output

Table 3.2.5.: General purpose I/O

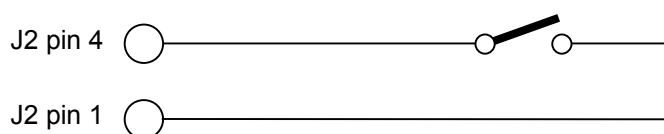
All bits of the output port are set to '1' by reset.

For more information see also the data sheet from MOTOROLA (MC68C681), EXAR (XR68C681) or PHILIPS (SCC68692).

4.2.6 MAX707 RESET AND BATTERY SUPERVISOR

The MAX707 is responsible for generating a correct reset after power up as well as to reset the CPU and its peripherals after the voltage drops below 4.65V. As a second task the MAX707 has to supervise the battery voltage of the external battery. If the voltage on the V_{Bat} input (J1/pin 5 and 6) drops below 2.2V a logical '0' can be read on IP5 of the DUART otherwise a logical '1' is present.

The MAX707 also supports a direct input for a reset switch. The switch can be connected in the following manner:



5. APPLICATION INFORMATION

5.1 ACCESSING ON BOARD FLASH

Since FLASH is not a memory like SRAM that can be written and read at any time in any block size (down to one byte) a special paragraph discusses the absolute basics that have to be known when working with this kind of memory.

5.1.1 FLASH ON THE VCM332

On the VCM332 FLASH is equipped as a word wide memory and can't be accessed on a byte per byte basis. It is implemented connecting two 8 bit wide chips in parallel, one on the lower and the other on the upper byte. This is essential especially for the programming algorithm, which must setup the FLASH chips for programming simultaneously on the lower and the upper byte lane. Type and manufacturer of FLASH's on the VCM332 are AT29C0x0 from Atmel.

5.1.1.1 PROGRAMMING THE FLASH CHIPS

Programming FLASH-Chips is not as easy as programming SRAM's. There exist several technologies with different programming schemes and protection mechanisms. To program FLASH's on the VCM332B/D it must be taken into account that one has to program an entire block of data. Data block sizes vary between the different memory sizes. Blocks to be written have to start at memory boundaries according to the block size. Following table lists these block sizes related to the Atmel part number:

MemSize	BlkSize	FLASH
256 kB	256 B	AT29C010
512 kB	512 B	AT29C020
1 MB	512 B	AT29C040A

NOTE

These Values are valid for the VCM332B/D board where two IC's are equipped.
Block and memory size of a single chip are only half the values in the table.

Further attention must be taken during sector write that the time between two word writes doesn't exceed 150µs. Otherwise programming of the memory cells starts before the entire block is written and unpredictable results will occur.

The architecture of the board doesn't allow single byte writes. Data has to be written in a word manner. Chip U11 is connected to data lines 7 to 0 while U13 connects to D15 to D8. Address line connection for both chips start with A1 (processor address line) to the FLASH pin marked A0.

After a complete block of data has been written, the chip internal programming algorithm starts with programming the memory cells. To determine if programming already has finished, the user has two different possibilities:

- 1) Reading back the last word written will result in inverted data on bits 7 and 15 as long as the chip is still in programming mode. After programming has finished, the correct word will be read back.
- 2) Successive attempts to read from the FLASH will result in toggling data lines 6 and 14. As soon as these lines don't toggle anymore the chip has finished programming.

5.1.1.2 READING THE FLASH

Reading from the FLASH is as easy as reading from SRAM. Just perform a move.w-instruction and you will get the correct data out of the FLASH.

5.2 OPTIMIZING PERFORMANCE

To be sure to operate at an optimum of performance it is essential to have a look at the hardware implementation and the software application.

5.2.1 HARDWARE DEPENDENT PERFORMANCE

Best performance on a given clock speed can be reached, if all of the connected memory and peripherals can be operated with zero wait states. Every wait state that has to be inserted at this clock frequency degrades possible performance.

Since the VCM332B/D is a complete single board computer, memory and peripherals are already present as described earlier in this manual. Needed wait states at given clock frequencies can be calculated for each functional block from the stated equations. One exception is the DUART on VCM332D modules. This peripheral chip is accessed asynchronously and has unpredictable response times. However an approximative equation can be taken to calculate wait state equivalents:

$$WS \geq (600ns / t_{CLK}) - 2$$

Where:

WS Wait state count
 t_{CLK} Processor clock period

5.2.2 PERFORMANCE DEPENDANCE FROM SOFTWARE

Software influences overall performance with the relative usage of the single functional blocks. Relative usage of a block is the percentage of accesses to that block compared to the total of accesses of the CPU. These values are highly application specific and have to be estimated for every project.

5.2.3 RELATIVE PERFORMANCE CALCULATION

To calculate relative performance following equation can be taken:

$$RP = 3 * f_{clk}/f_{max} * [RU_{SRAM}/(3+WS_{SRAM}) + RU_{FLASH}/(3+WS_{FLASH}) + RU_{EPROM}/(3+WS_{EPROM}) + RU_{DUART}/(3+WS_{DUART}) + RU_{RTC}/(3+WS_{RTC})]$$

Where:

RP Relative Performance (in percent)
 RU Relative Usage of the individual blocks (in percent)
 WS Wait States of the individual Blocks

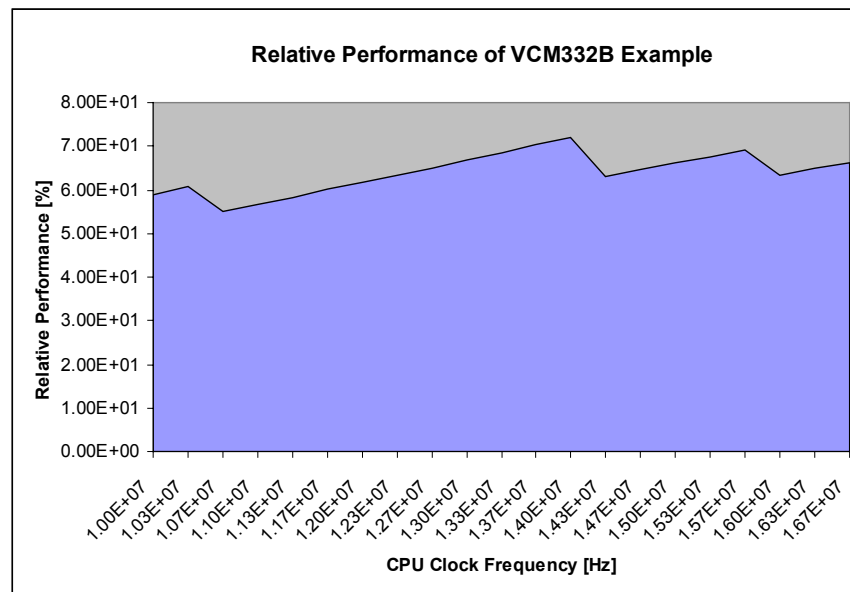
If the VCM332 is to be supplemented with application specific hardware, terms of the kind $RU/(3+WS)$ can be added for each functional block.

5.2.3.1 EXAMPLE OF RELATIVE PERFORMANCE CHART

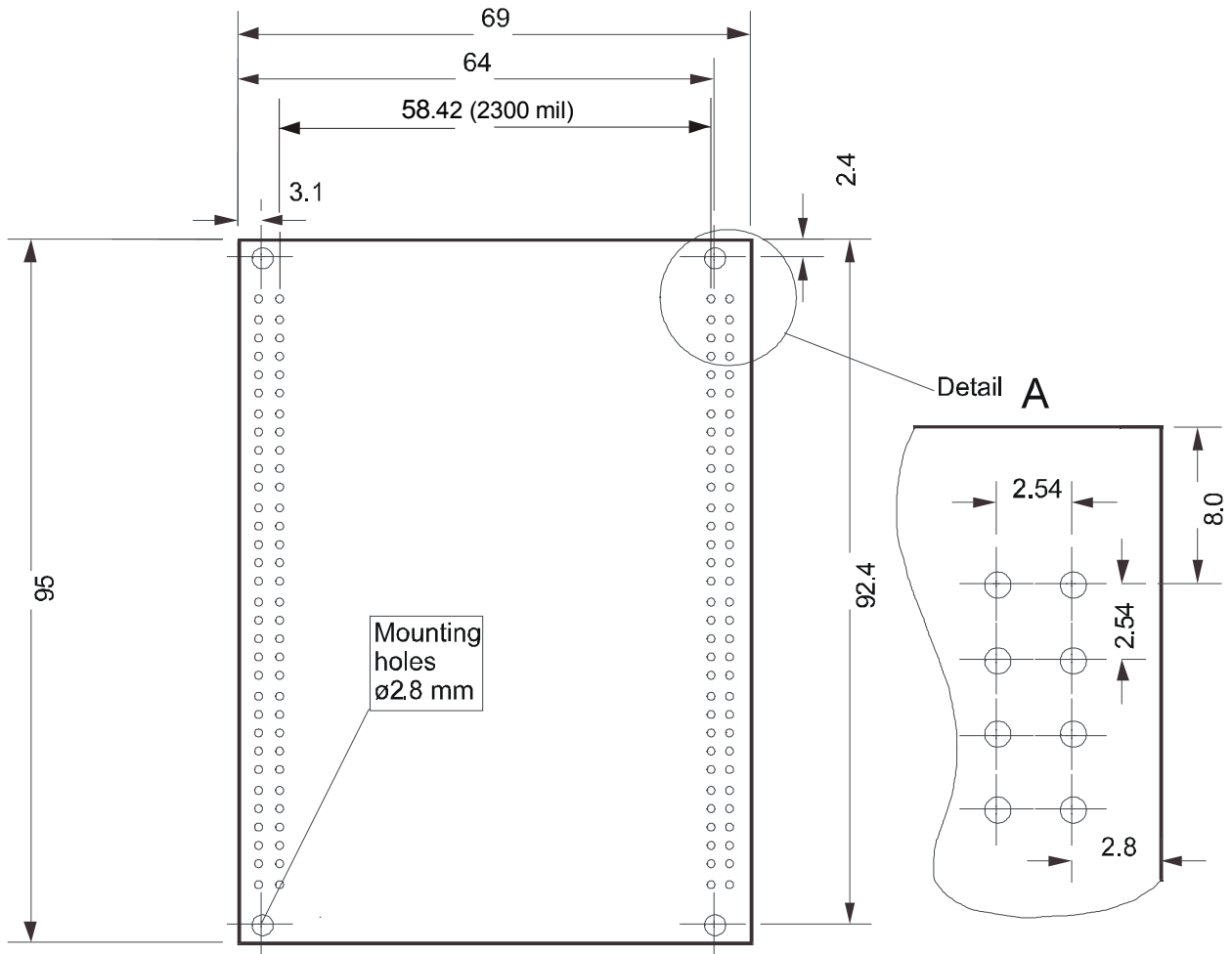
To give an example of relative performance of a VCM332B let us assume the following:

RU _{SRAM}	49%	SRAM is used as variable storage
RU _{EPROM}	0%	No EPROM is equipped
RU _{FLASH}	49%	FLASH is used as boot and program execution memory
RU _{DUART}	1.5%	We have some serial traffic
RU _{RTC}	0.5%	The RTC is used

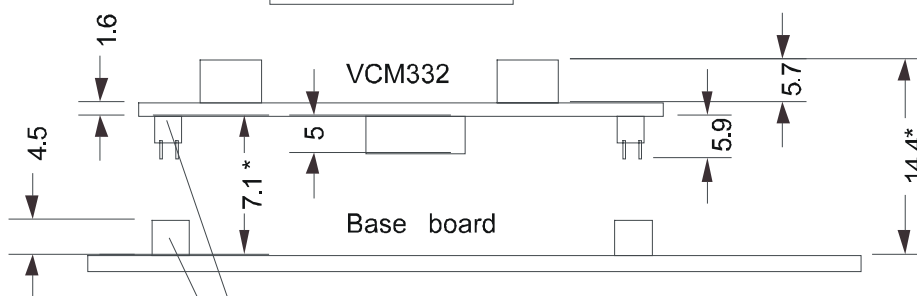
The following performance chart results:



This shows, that under the assumed conditions we have a maximum performance if the VCM332 is run at about 14 MHz and not if it is run at 16.77 MHz!



All Units in mm



*These measurements refer to the connectors below (put together).

Connectors:

Male: Comatel No. 473 0543-1-64-400 (2x1 pc.)
 Female: Comatel No. 477 3001-1-16-400 (2x4 pc.)

Fig. 4: Mechanical dimensions

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