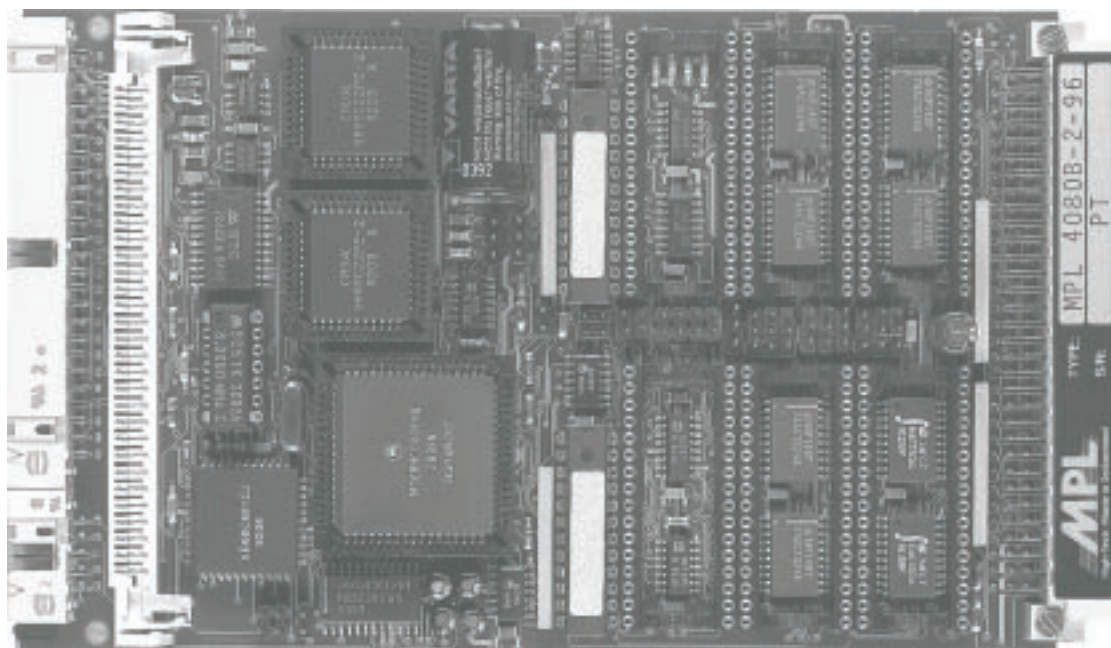


HIGH FUNCTIONALITY CMOS 68000 SINGLE BOARD COMPUTER

The MPL 4080B is the industry's most integrated, all CMOS 68HC000 16/32-bit single board computer, and has an impressive list of features: six 32-pin sockets for SRAM/EPROM or EEPROM, on-board battery for buffering of SRAM and RTC, serial and parallel I/O's, Real Time Clock with calendar, Watchdog and Power fail detection, and serial EEPROM. The MPL 4080B can be further customized with the use of a miniature 30-pin connector for additional mounting of SIMM Modules (small PCBs). The board also supports a full 16-Bit G-64/G-96 bus interface for I/O extension and up to 12 Mbytes of external memory. The fully CMOS architecture and its single-supply design draws a mere 100mA at 5V and makes the MPL 4080B ideal for a wide range of control, data acquisition, and portable microcomputer applications.

TECHNICAL FEATURES

- Powerful 16/32-bit 68HC000
- 8 MHz clock (10, 12.5, 16 MHz optional)
- Six sockets for up to 3 Mbytes of SRAM/EPROM
- Up to 2 Mbytes of battery buffered SRAM
- JEDEC pin-out for 4 Mbit SRAM devices
- Up to 2 Mbytes of EPROM
- Up to 256K of EEPROM
- 1024 bit serial EEPROM included
- Two programmable RS-232 serial ports
- 40 TTL I/O lines
- Five 16-bit timers
- Real-time clock with calendar
- Powerfail detection
- Watchdog
- Full G-64/G-96 bus interface
- External memory expandable to 12 Mbytes
- Supports sync. and async. I/O transfers
- Bus arbitration capability
- On-board MLX SIMM local extension bus
- On-board DC/DC converter for single 5V supply
- All CMOS design
- Very low power consumption: 95mA typ. at 5V only
- Compact single height Eurocard design (100 x 160 mm)
- 4-level multilayer design
- Comprehensive software support
- Available in extended temperature range



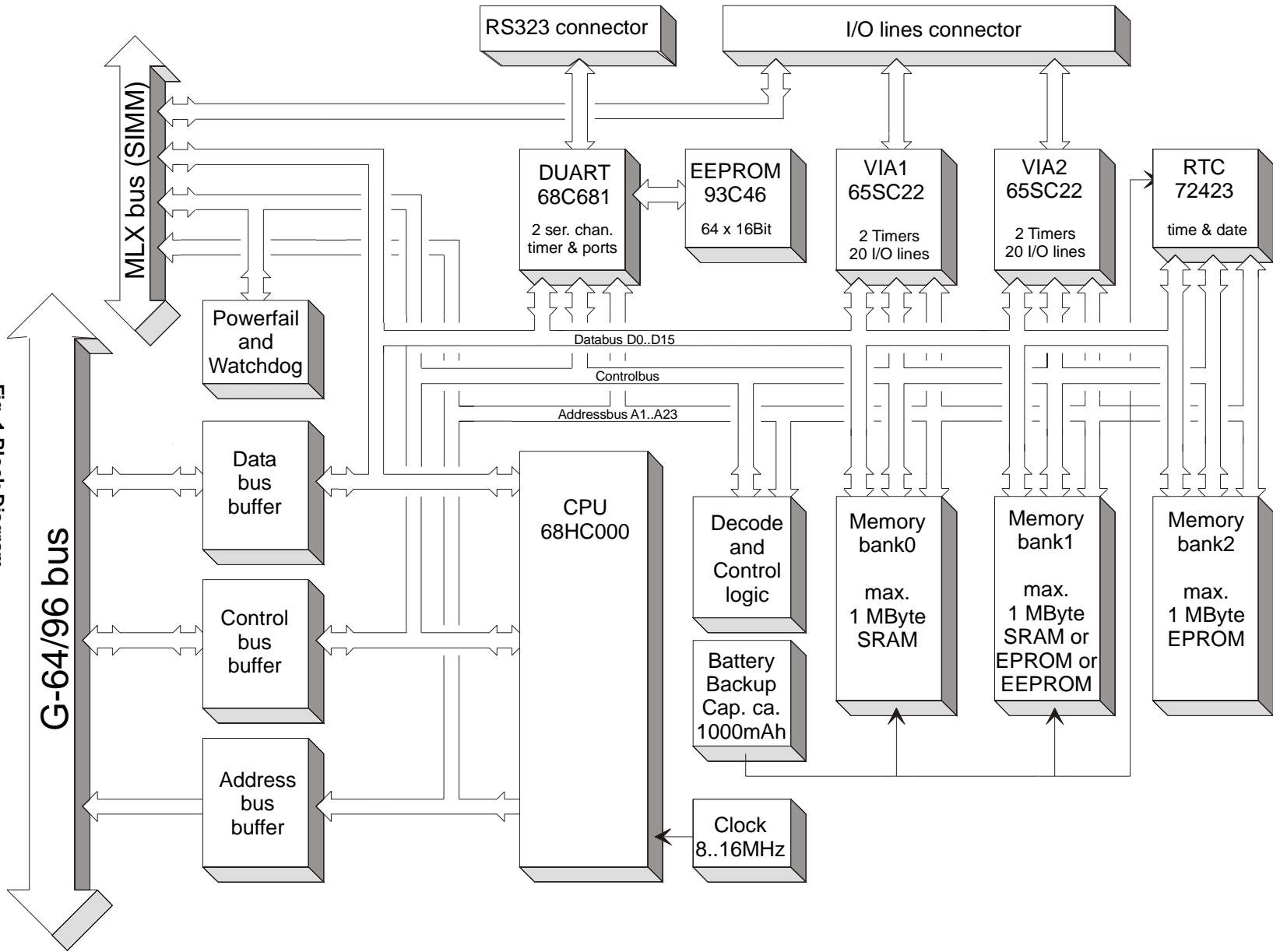
References

- MPL 4080B-2: High functionality CMOS 68000 single board computer
 MPL 4080B-2X: ditto in extended temperature -25 to +85 °C

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Fig. 1 Block Diagram



1. GENERAL INFORMATION

1.1 DESCRIPTION

The MPL 4080B is a high density single board computer, built in all CMOS low power technology around a 16/32 Bit MC68HC000 running at 8 MHz (with higher speeds available as an option). The MPL 4080B is loaded with features that make it one of the most powerful and most versatile single board computers in the market. The board contains six JEDEC sockets that can be equipped with up to 3 Mbytes of SRAM/ EPROM. The SRAM is battery backed using an on-board lithium battery. A 1024 bit serial access EEPROM allows the permanent storage of useful operating parameters. In addition, the MPL 4080B is equipped with two RS-232 serial ports, 40 TTL I/O lines, five 16 Bit timers, a Real Time Clock with calendar, and a Power-fail detection and Watchdog circuit. An on-board DC/DC converter is provided for the RS-232 drivers while using a single 5V supply for the board.

For additional memory and I/O, the board can be extended, through its G-64 bus interface, up to 12 Mbytes. The G-64 bus is a favourite 16/32-bit bus architecture among OEMs of embedded computer systems. An exciting feature of the MPL 4080B is its use of a 30 pin. SIMM (Single Inline Multipurpose Module) microedge connector to accept small PCBs mounted at a 30 degree angle for the purpose of installing additional I/O to the board. All relevant signals to operate 8 bit peripherals are available on that connector. MPL AG is offering a line of SIMM add-on modules. Available today (Jan. 93) is a module containing a 12-bit A/D and D/A converter, three serial modules covering different customer needs and a CAN (Controller Area Network) module.

Software development on the MPL 4080B is simplified by the availability of the OS-9 real-time, multitasking operating system. MPL AG also supplies software allowing cross development for the MPL 4080B using an IBM PC. The MPL 4080B fills an important need for high performance, ruggedized extended temperature, low power microcomputer systems for application in transit systems, portable instruments and testers, and remote data acquisition systems.

1.2 TECHNICAL CHARACTERISTICS

Processor: Processor clock:	68HC000 8 MHz clock (10, 12.5, 16 MHz optional)
Memory: No JEDEC sockets: Max. Memory:	6 x 32-pin 3 Mbytes Up to 2 Mbytes SRAM Up to 2 Mbytes EPROM Up to 256 Kbytes EEPROM 1024 Bit serial EEPROM
Equipped memory:	
Serial ports: No of ports: Baud rate:	Two RS-232C (68C681) 50 - 38400, software programmable
TTL I/O:	40 digital I/O lines with TTL-Level (two 65SC22)
Clock/timers: Timers: Clock/Calendar:	Five 16-Bit timers RTC72423, battery backed
Bus interface: Interface type: Ext. Mem. Addressing: Memory transfers: I/O Addressing: I/O transfers: Enable clock: Bus arbitration:	Full G-64/G-96 12 Mbytes (VMA) Asynchronous 1 kWord (VPA) Sync./Async. CPU clock / 10 Supported
G-96 Interrupts:	3 auto-vectored 2 vectored
Local Expansion: Bus Name: Connector type: Bus Type:	(MLX) Mpl Local eXpansion 30-pin SIMM 8-bit synchronous
Board Dimensions:	Single Eurocard (100 x 160mm)
Technology:	100% CMOS Surface Mounted Devices
Power requirements: Power range:	+ 5V only / 95mA with SRAM/EPROM (8 MHz) 4.80V - 5.25V On board DC/DC-converter for RS-232C
Temperature range: MPL 4080-X version: On request:	0° to +70°C (+32° to +158°F) -25° to +85°C (-13° to +185°F) -40° to +85°C (-40° to +185°F)
Relative humidity:	20-90% non condensing

1.3 POWER CONSUMPTION

The fully CMOS-design of the MPL 4080B results in a low power consumption. The power values have been determined in a configuration similar to a single board application with following parameters: Supply of 5.0 volts, ambient temperature +25° C, fully equipped, four 1 Mbit CMOS SRAMs and two 1 Mbit EPROMs, 8 MHz CPU clock, serial communication on one channel, but the MPL 4080B is *not* mounted on a back-plane. The measured values were:

CPU 100% idle:	typ. 70mA
CPU 100% processing:	typ. 95mA

Note that at lower temperatures (-25°C) there will be an additional current consumption of approx. +15mA. At higher temperatures (+85°C) the consumption decreases by approx. -15mA. Likewise, increasing the CPU clock frequency increases the consumption. The rule of thumb for the MPL 4080B is: +5-6mA per MHz.

1.4 DIFFERENCES TO THE MPL 4080

This paragraph is intended for users that are familiar with the MPL 4080.

The new MPL 4080B described in this manual is an upgrade to the MPL 4080. The main purpose to this upgrade was to make it possible to utilise 4 Mbit chips. At the same line some other changes were implemented. Transforming software running on the MPL 4080 to the MPL 4080B is just the matter of a few minutes.

The following features of the MPL 4080B are different to those of the MPL 4080:

- **Memory map.** A new memory map was introduced since the on-board memory capacity had been extended (4 Mbit SRAMs/ EPROMs can be used). The on-board memory capacity is raised from 768 KByte to 3 MByte in total. As a consequence, the external memory capacity (G-96 VMA) had to be lowered from 15 Mbyte to 12 MByte. However, the structure of the memory map is still identical to the one of the MPL 4080. Please refer to paragraph 3.2.

- **Some jumpers.** Almost all jumpers have the same function, same orientation and same location as on the MPL 4080. The only exceptions are:

- Jumpers J8, J9, J10 and J11. They are used to select type and size of the on-board memory. Refer to paragraphs 2.3.3 - 2.3.6.
- Jumper J16. The new definition is inverse to the old one: IP4 and IP5 are swapped. Refer to paragraph 2.3.13.

- **Optional chip LEDs.** On the solder side of the MPL 4080B, two chip LEDs can be mounted. They are driven via DUART output ports OP5 and OP6. Refer to paragraphs 2.5.2 and 3.3.3.

- **G-96 interface.** The G-96 reset output is now an open collector output but still not bi-directional.

- **G-96 bus line 28c (ARBCLK)** is open now (no longer supplied with the system clock).

- **Power consumption.** The power consumption is reduced by approx. 25mA. The MPL 4080B draws 95mA typically (at 8 MHz), compared to the MPL 4080 that draws 120mA.

- **Cosmetic.** Mild 'cosmetics' have been applied to the board. Especially the packaging style of some ICs have been changed from dual-in-line to surface mount. This means the MPL 4080B looks slightly different to the MPL 4080, but without any further electrical changes.

2. PREPARATION FOR USE, INTERCONNECTION

2.1 PARTS LOCATION

The diagram of Fig. 2.1 shows the position of all components, jumpers and connectors on the MPL 4080B.

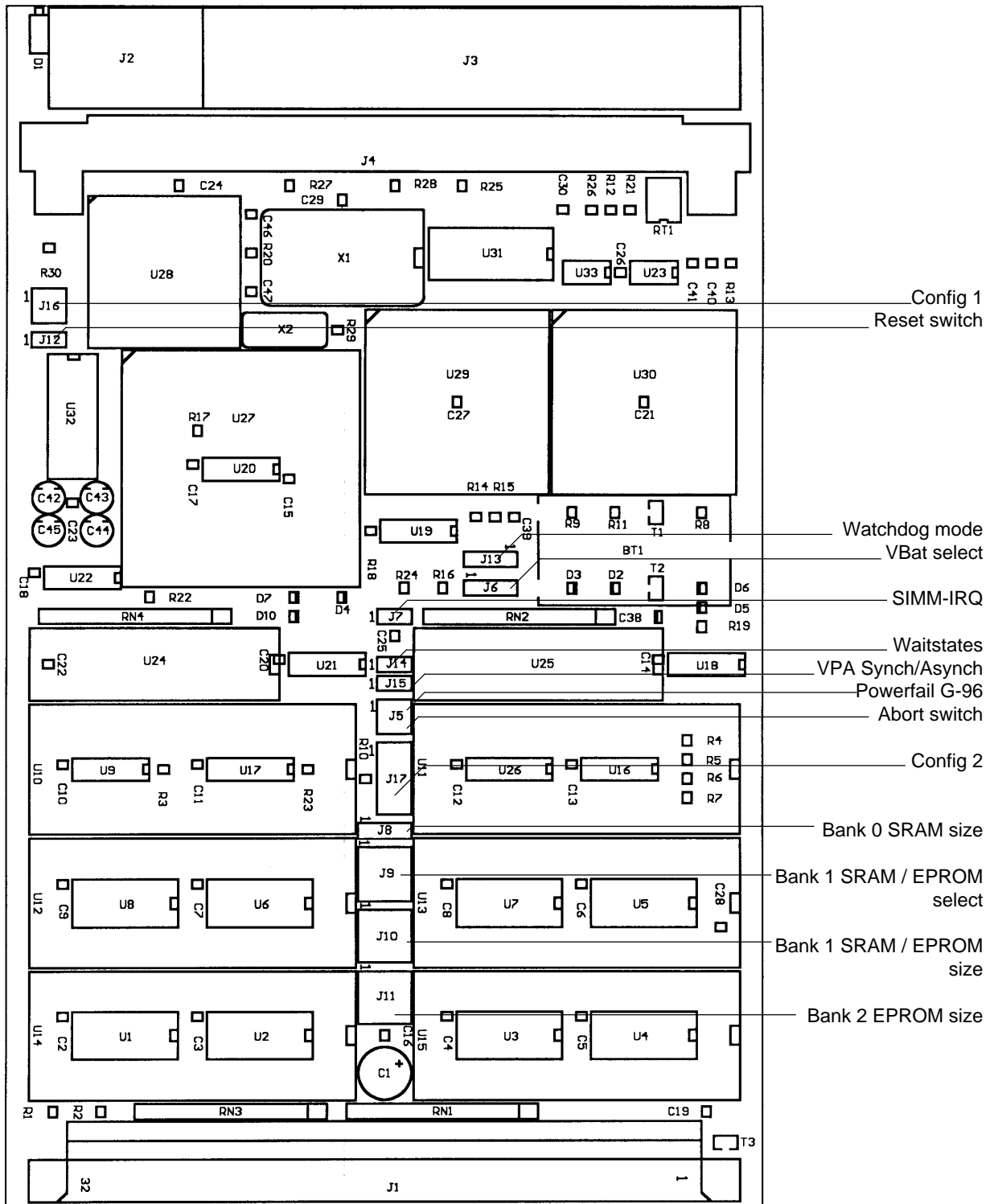


Fig. 2.1 MPL 4080B parts location

2.1.1 JUMPER AND CONNECTOR OVERVIEW

Name	Function
J1	G-96 connector
J2	Dual RS-232 connector
J3	I/O lines connector
J4	SIMM microedge connector
J5	Abort/PWF-G-96 jumper
J6	Battery source selection and back-up of bank 0 and RTC
J7	SIMM Module interrupt
J8	Size of SRAM on bank 0
J9	Type of memory on bank 1 and battery backup
J10	Size of memory on bank 1
J11	Size of EPROM on bank 2
J12	Reset
J13	Soft-/hardware clear of the watchdog
J14	On-board memory wait states
J15	Selecting sync. / async. G-96 VPA-range
J16	Configuration 1 (2 Bit)
J17	Configuration 2 (4 Bit)

Table 2.1.1 Jumper and connector assignment

2.2 ABOUT MEMORY AND BANKS

The universality of the memory space makes some preceding information necessary.

2.2.1 MEMORY BANKS

There are three memory banks. Each bank consists of two 32 pin sockets and is split in a LOW and a HIGH byte. Locate the below mentioned part names in Table 2.2.1

	Low byte (D0 - D7)	High byte (D8 - D15)	Mountable type of memory
Bank 0	U10	U11	SRAM
Bank 1	U12	U13	SRAM or EPROM or EEPROM
Bank 2	U14	U15	EPROM

Table 2.2.1 Location and memory types

2.2.2 HOW TO USE MEMORY BANK 0 - 2

It is important to read this paragraph before commencing to insert memory into the sockets of the three banks. It details what type of memory and which sizes are mountable (selectable with jumpers J8, J9, J10 and J11). SRAM/(E)EPROM device-sizes from 256 kbit to 4 Mbit (in byte organization) can be mounted on all three memory banks. The following table defines the usable device-sizes:

	Type of memory	Usable memory sizes
Bank 0	SRAM	256K / 1M / 2M / 4Mbit
Bank 1	SRAM EPROM EEPROM	256K / 1M / 2M / 4Mbit 256K / 512K / 1M / 2M / 4Mbit 64K / 256Kbit
Bank 2	EPROM	256K / 512K / 1M / 2M / 4Mbit

Table 2.2.2 Minimum and maximum memory sizes

Notes:

- Bank 0 and bank 1 can be battery backed. Bank 1 can be battery backed only if bank 0 is backed, too.
- Use low power SRAMs (CMOS) in case of battery backing.
- 2 Mbit SRAMs are not being manufactured as monolithic chips but 2 Mbit SRAM modules with a JEDEC compatible pin out are available (i.e. Dense-Pac DSP256S8P or EDI8M8257LP).
- If EPROM or EEPROM is plugged into bank 1, ensure that the battery back-up for bank 1 is NOT SET. Otherwise the battery can be discharged prematurely.
- If you use 1 Mbit EPROMs be sure to use JEDEC-types. There are EPROMs available with a Mask ROM compatible pin out which is not compatible to the JEDEC pin out (examples of these incompatible MaskROM versions are i.e. NEC27C1000, TC571001, Am27C100). These types are not supported by the MPL 4080B.
- The use of EEPROMs (no FlashROMs!) in bank 1 is subject to some restrictions.
 - EEPROMs with a RDY/BSY-Output can be used, but the output can not be read. For that reason, the EEPROMs should have a Data Polling feature to detect the completion of the internal write-cycle.
 - To guarantee correct write-cycles, the EEPROMs have to be of 'Chip Select' controlled write-cycle-type. Worst case calculations for faster CPU speeds (more than 12.5 MHz) point to a potential timing problem at the 'Chip Select Hold'- and the 'Output Enable Hold'- time. Measurements even at extended temperatures and 16 MHz however showed a uncritical timing scheme.

2.2.3 MEMORY ACCESS TIME

The access time of the internal memory is determined by the CPU clock frequency and the number of wait states included in read and write accesses. On the MPL 4080B, the access logic treats read and write accesses the same way and supports real 'zero wait states'. This means: When set to 'zero wait states', both read and write accesses are terminated on the falling edge of state S6 of the processor timing. Setting 'one wait state' inserts one extra CPU-cycle in read and write accesses.

Wait states	Worst case Memory access time for different CPU frequencies			
	8 MHz	10 MHz	12.5 MHz	16 MHz
0	185ns (250ns)	135ns (200ns)	100ns (150ns)	85ns (120ns)
1	310ns (400ns)	235ns (300ns)	180ns (250ns)	150ns (200ns)

Table 2.2.3 Required speed of memory devices

The values in parenthesis denote 'real' access times. With our experience, memory devices with access times as indicated in parenthesis are sufficient even in extended temperature applications.

2.2.4 MEMORY PIN ASSIGNMENT (U10 - U15)

Memory chips in 28-pin DIL packages must be bottom-aligned (pin 1 of the chip meets pin 3 of the socket).

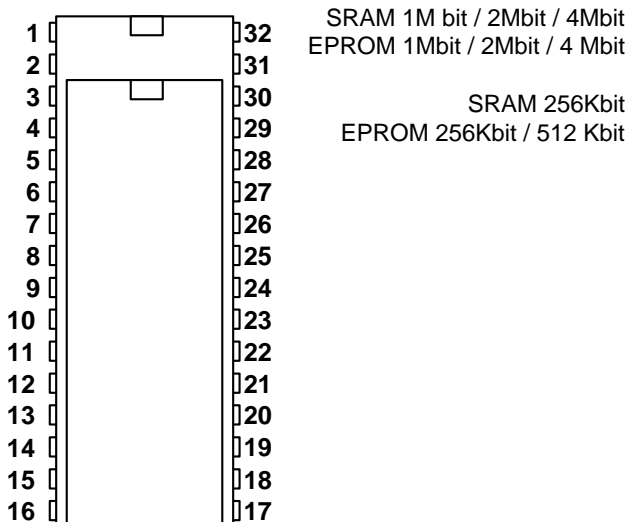


Fig. 2.2.4 Memory pin assignment

2.3 JUMPER CONFIGURATION AND DESCRIPTION

A lot of functions are implemented on the MPL 4080B. Some of these functions have to be set, enabled or disabled by means of jumpers. The locations, the different valid combinations and the meaning of the jumpers are given in the following paragraphs.

2.3.1 JUMPER ORIENTATION

A special feature of the MPL 4080B helps to check misplaced jumpers: Each jumper placed to its position has to be parallel to the G-96 connector (this does not exclude additional mis-jumpering).

2.3.2 BATTERY SOURCE SELECTION AND BACKUP OF BANK 0 AND RTC (J6)

Installing jumper J6 in either position enables the battery buffering for bank 0 and the RTC at power-down situations. Battery backup of bank 1 is not yet active, it needs additional jumpering, see 2.3.4. The two possible battery power sources are the on-board lithium battery or a battery connected to the corresponding G-64/96 bus line. If no battery buffering is required, jumper J6 should be removed.

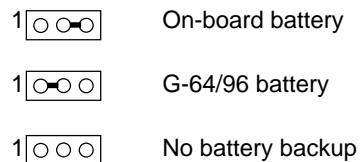


Fig. 2.3.2 Battery buffering bank 0 and RTC

2.3.3 SIZE OF SRAM ON BANK 0 (J8)

Memory bank 0 can be equipped with SRAM only. The size of the SRAM devices is defined by jumper J8.

- 1 256 kbit / 1 Mbit
- 1 2 Mbit / 4 Mbit

Fig. 2.3.3 Bank 0 SRAM size selection

2.3.4 TYPE OF MEMORY ON BANK 1 AND BATTERY BACKUP (J9)

Bank 1 can be equipped with SRAM, EEPROM or EPROM of sizes from 256 kbit to 4 Mbit. Jumper J9 sets the type of memory (SRAM or EPROM).

If SRAM is used, the battery backup can also be defined by jumper J9, but battery backup is activated only if a battery source had been selected on jumper J6.

- 1 SRAM with battery backup (of any size)
- 1 EEPROM or SRAM without battery backup (of any size)
- 1 EPROM (of any size)

Fig. 2.3.4 Bank 1 memory type selection

2.3.5 SIZE OF MEMORY ON BANK 1 (J10)

After having selected the type of memory on J9, the size of the memory has to be defined on jumper J10. The following drawings show the various jumper configurations.

- 1 EEPROM 64 kbit (with or without RDY/BSY-Out.)
- 1 SRAM 256 Kbit / 1 Mbit
EEPROM 256 Kbit
- 1 SRAM 2 Mbit / 4 Mbit

- 1 EPROM 256 kbit

- 1 EPROM 512 kbit / 1 Mbit

- 1 EPROM 2 Mbit

- 1 EPROM 4 Mbit

Fig. 2.3.5 Bank 1 memory size selection

2.3.6 SIZE OF EPROM ON BANK 2 (J11)

Bank 2 accepts five different EPROM-sizes. They have to be set as illustrated below.

- 1 EPROM 256 kbit

- 1 EPROM 512 kbit / 1Mbit

- 1 EPROM 2 Mbit

- 1 EPROM 4 Mbit

Fig. 2.3.6 Bank 2 EPROM size selection

2.3.7 ABORT/PWF-G96 JUMPER (J5)

This 2x2 jumper field has two functions. If a jumper is installed in the upper position as shown below, an active low signal on the G-96 powerfail line releases a level 7 interrupt (NMI). An external abort switch can be connected to the lower position. A closure on this switch will also cause a level 7 interrupt.

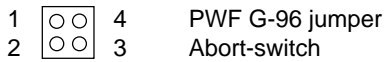


Fig. 2.3.7 Abort- and PWF-jumper

2.3.8 SIMM MODULE INTERRUPT (J7)

The SIMM microedge connector (MLX-bus) provides an active low interrupt output line. This line is internally connected to interrupt level 4 (together with VIA1 and VIA2) and at the same time to the DUART input port 3 ('IRQ-Flag'). Jumper J7 offers the possibility of disconnecting the SIMM Module interrupt from interrupt level 4 by removing the jumper. The IRQ-Flag bit at the DUART input port is still available.

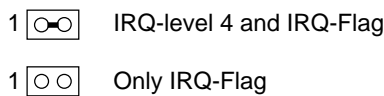


Fig. 2.3.8 Jumper J7

2.3.9 RESET (J12)

J12 allows to connect an external reset (restart) switch. A closure on this switch releases a RESET that will be active over the whole system.



Fig. 2.3.9 Reset switch

2.3.10 SOFTWARE / HARDWARE CLEAR OF THE WATCHDOG (J13)

The watchdog can be jumpered to be cleared by a periodic hardware signal (watchdog is disabled) or under software control (watchdog is enabled).

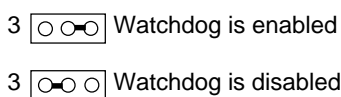


Fig. 2.3.10 Watchdog clear

2.3.11 ON-BOARD MEMORY WAIT STATES (J14)

On the MPL 4080B, two different wait states can be jumpered by J14 (see also 2.2.3). The selection is valid only for an access to memory banks 0 - 2.

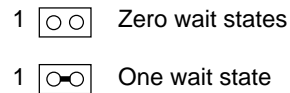


Fig. 2.3.11 Wait state selection

2.3.12 SELECTING SYNC. OR ASYNC. G-96 VPA-RANGE (J15)

The lower half of the G-64/96 VPA-range (500 words) is accessible only in the synchronous mode. Access to the upper 500 words can be jumpered to be synchronous or asynchronous.

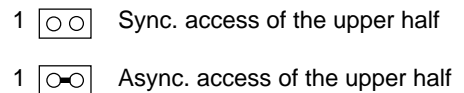


Fig. 2.3.12 Sync./async. selection of the VPA-range

2.3.13 CONFIGURATION 1 (J16)

A 2-Bit configuration can be set and read via DUART input ports 4 and 5. A jumper set will be read as a '0', a jumper left open will be read as a '1'.

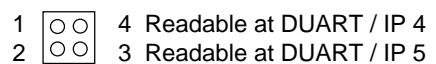


Fig. 2.3.13 Configuration 1

2.3.14 CONFIGURATION 2 (J17)

A 4-Bit configuration can be set and read (via data lines D0 - D3).

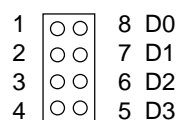


Fig. 2.3.14 Configuration 2

2.4. CONNECTORS

2.4.1 LOCAL EXTENSION BUS (J4)

The MPL 4080B is equipped with a 30-pin SIMM microconnector for the installation of small and low cost peripheral devices. See chapter 4 for complete details on the local extension bus specifications.

2.4.2 DUAL RS-232 CONNECTOR (J2)

J2 allows the connection of two serial channels with hardware handshake. The communication device on the MPL 4080B is a DUART 68C681. All RS-232 output signals have a typical voltage range of ± 9 Volts. The following table shows the pin-out of the 10-pin connector.

Pin	Signal
1	TxD A
2	RxD A
3	RTS A
4	CTS A
5	GND
6	TxD B
7	RxD B
8	RTS B
9	CTS B
10	GND

Table 2.4.2 RS-232 connector

Suffix "A" denotes Channel A, suffix "B" denotes channel B. "A" and "B" correspond to the denotation used in the device data sheet of the communication controller 68C681.

2.4.3 I/O LINES CONNECTOR (J3)

J3 is a 50-pin connector with 40 VIA I/O lines (four VIA-Ports including all handshake signals), 8 SIMM Module I/O lines and 1 VCC- and 1 GND-line. Table 2.4.3 shows the pin out of connector J3. Pins 1 to 20 are the I/Os of VIA1 (U29), pins 21 to 40 are the I/Os of VIA2 (U30) .

Pin number	Signal	Pin number	Signal
1,21	PA0,PA0	16,36	PB5,PB5
2,22	PA1,PA1	17,37	PB6,PB6
3,23	PA2,PA2	18,38	PB7,PB7
4,24	PA3,PA3	19,39	CB1,CB1
5,25	PA4,PA4	20,40	CB2,CB2
6,26	PA5,PA5	41	SIMM2
7,27	PA6,PA6	42	SIMM3
8,28	PA7,PA7	43	SIMM4
9,29	CA1,CA1	44	SIMM5
10,30	CA2,CA2	45	SIMM6
11,31	PB0,PB0	46	SIMM7
12,32	PB1,PB1	47	SIMM8
13,33	PB2,PB2	48	SIMM9
14,34	PB3,PB3	49	VCC(+5V)
15,35	PB4,PB4	50	GND

Table 2.4.3 I/O lines connector

2.5 INDICATORS

2.5.1 STATUS LED

The MPL 4080B provides a status indicator LED. Whenever the indicator is "on", something is wrong.

The red LED D1 will be on permanently if:

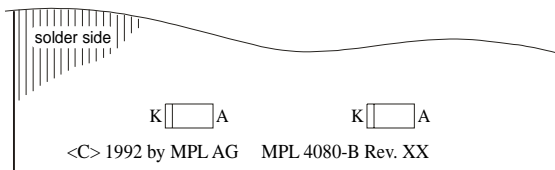
- the power (VCC) in power-up never exceeds 4.80V
- the power (after a correct power-up) drops below approx. 4.60V
- the microprocessor is in the HALT-state (i.e. double bus error or HALT G-96)

The LED will periodically turn on (RESET) and off with approx. 4 Hz, if the watchdog time out had been released as a result of a missing clear signal (see 3.3.1).

2.5.2 OPTIONAL LEDS

On the solder side of the MPL 4080B two chip LEDs can be mounted (located at the upper card edge, above the string "<c>1992 by MPL AG").

For each LED a series resistor of 330 is already provided. This results in a diode forward current of approx. 8mA. The LEDs are controlled by the DUART 68C681 outputs OP5 and OP6. Programming an output to "0" lights the corresponding LED. See Fig 2.5.2 for details and read paragraph 3.3.3 for the bit definition of the DUART output port.



Connected to DUART: OP6

OP5

Fig 2.5.2 LEDs (optional)

Note:

Chip LEDs with almost equal luminous intensities are available from Citiled (example): CL-150SR (red), CL-150Y (yellow), CL-150FG (fresh green).

3. OPERATION

3.1 BASIS

This section outlines some basic operation and function principals of the MPL 4080B.

3.1.1 MEMORY BANK 0 SWITCHING

During normal operation the SRAM starts at address \$0. After reset the memory bank 2 (EPROM) is fade in at address \$0 to define the exception vectors (especially initial PC and SSP). For normal operation this 'EPROM fade in' has to be disabled. This is done by programming the DUART OP7 (Output Port 7, pin 17) to go low (the pin is high after reset).

Please study the following programming example:

```
RamEnd    equ    $FFFFFF    for two 4 Mbit SRAM chips
ACPortA   equ    $300401    base address of
*          *                DUART 68C681
MPSOPCR   equ    $1A        68C681 Output Port
*          *                Config Register
MPSOPort  equ    $1C        68C681 Output Port
*          *                Set Register
```

**** Here starts EPROM for memory bank 2 ****

```
org       $200000
dc.l     RamEnd           initial SSP
dc.l     start            initial PC

start    movea.l #ACPortA,a3    get 68C681 base
*          *                address
*          *                move.b # $00,MPSOPCR(a3)    output ports 2 to 7
*          *                *                are outputs
*          *                *                move.b # $80,MPSOPort(a3)    output port 7 to low
*          *                *                -> EPROM fade in
*          *                *                is disabled
*          *                *                move.l $200000,$0        copy stack pointer
*          *                *                to RAM
*          *                *                move.l $200004,$4        copy reset vector
*          *                *                to RAM
```

Table 3.1.1 Programming example

3.1.2 ASYNC. VS SYNC. OPERATION

The MPL 4080B supports both asynchronous and synchronous data transfer between CPU and memory/peripheral. Asynchronous transfers need to be terminated by a data acknowledgement signal (DTACK). Read-Modify-Write cycles are correctly supported in both asynchronous and synchronous mode.

All transfer modes supported on the MPL 4080B are listed in table 3.1.2.

Device	Data transfer	DTACK origin
Memory	asynchronous	on-board
DUART	asynchronous	on-board
VIAs	synchronous	--
RTC	synchronous	--
SIMM Module	synchronous	--
G-64/96 VPA	sync. and/or async.	external (async.)
G-64/96 VMA	asynchronous	external

Table 3.1.2 Operational modes

3.1.3 INTERRUPT LOGIC

The relation between interrupt source, interrupt mode and interrupt level is hard-wired and cannot be altered. Interrupt levels 1 to 6 are level sensitive while level 7 is transition sensitive.

Level	Mode	Source
1	auto-vect.	G-64/96 IRQ1 (or G-64 IRQ)
2	auto-vect.	G-64/96 IRQ2 (or G-64 FIRQ)
3	vectored	G-96 IRQ3
4	auto-vect.	VIA1 & VIA2 & SIMM Module
5	vectored	G-96 IRQ5
6	vectored	DUART 68C681
7	auto-vect.	Power Fail MPL 4080B NMI G-64/96 Abort Switch Power Fail G-64/96 (enable/disable by jumper)

Table 3.1.3 Interrupt logic

3.1.4 ADDRESSING OF 8-BIT PERIPHERAL DEVICES

Pay attention when accessing on-board peripherals: On the MPL 4080B, all peripheral devices are 8-bit wide and connected to the lower data byte (D7 - D0) of the CPU data bus but are addressed as 16-bit ports. Therefore use odd addresses only and increment the address by 2 to get the next contiguous address.

Accessing 8-bit peripherals via the G-64/96 bus is similar. These peripherals are internally connected to the lower data byte (D7 - D0, odd) or the higher data byte (D15 - D8, even). In each case, increment the address by 2 to get the next contiguous address.

3.1.5 BUS ERROR LOGIC

In a 68HC000 system, each asynchronous access to any peripheral or memory device has to be terminated by an acknowledgment signal (/DTACK). The device itself or a special decode logic has to deliver this acknowledgment, otherwise the microprocessor will forever hold the initiated bus cycle active. To prevent this, an on-board bus error logic aborts such a data transfer after approx. 20µsec and releases a bus error (BERR).

Note:

On the MPL 4080B the BERR signal is not accompanied by a HALT signal. Thus the 68HC000 will not initiate a rerun bus cycle. The bus error has to be handled in software. A renewed bus errors during the exception processing will be treated as a catastrophic error (double bus fault) and the 68HC000 will automatically enter the HALT-state and remain there until reset.

3.2 MEMORY MAP

The following table shows the memory map.

Addresses	Addresses on G-96 bus (1)	High Byte (D15 - D8, even)	Low Byte (D7 - D0, odd)	Sync./Async.	Comments
FFFFFF 400000	7FFFFFF 200000	VMA G-64/96		Async.	
3304BF 3304A0			Configuration 2	Sync.	See (2),(3)
33049F 330480			SIMM Module	Sync.	
33047F 330460			VIA2	Sync.	
33045F 330440			VIA1	Sync.	
33043F 330420			Watchdog	Sync.	
33041F 330400			RTC	Sync.	see (3)
3207FF 320400	1903FF 190200	VPA G-64/96		Sync. or Async.	selectable
3203FF 320000	1901FF 190000	VPA G-64/96		Sync.	
3007FF 300400			DUART	Async.	
2FFFFFF 200000		EPROM (Bank 2)		Async.	
1FFFFFF 100000		SRAM/EPROM (Bank 1)		Async.	
0FFFFFF 000000		SRAM (Bank 0)		Async.	See (4)

Table 3.2 Memory map

Notes:

- (1) CPU address lines A1 - A23 drive the G-96 address bus lines A0-A22 (bus line A23 is always low). Thus a G-64/96 access is actually a word-access. Seen on the G-64/96 bus, the addresses are divided by two. The effective bus addresses are listed in this column.
- (2) Reads configuration at J17
- (3) Only data lines D0 - D3 are used
- (4) After reset an access to memory range 000000...0FFFFFF (bank 0) is actually an access to memory range 200000 - 2FFFFFF (bank 2). See also paragraph 3.1.1.

3.3 DEVICE DESCRIPTION

In this section, the interfaces and devices of the MPL 4080B will be described. Sometimes you will find the sentence "see the data sheet.....for more information". These data sheets will usually give you more accurate information about the circuits than could possibly be given within the scope of this manual.

3.3.1 WATCHDOG (U23)

If the watchdog is enabled, it must be reset periodically to prevent watchdog time-out and system reset. The watchdog is reset (cleared) by a read or write access (TCL) to the corresponding address. If the watchdog is not cleared within the time out period (T_{to}) of 100ms, a system reset will be performed. After an additional 100ms, reset will be withdrawn (inactive) to give the system a chance to perform a renewed start-up. This sequence will be repeated periodically until the watchdog is cleared again. See Fig. 3.3.2 for details.

3.3.2 POWERFAIL (U23)

To guarantee correct operation of the MPL 4080B after power-up, the power (VCC) has to rise above 4.80V. Otherwise the system reset will stay active. In power-down (powerfail situation) the MPL 4080B will run through the following stages:
 4.70V: When the power drops below this voltage level, a powerfail monitor releases a level 7 interrupt (NMI). This gives the possibility of saving data to a battery buffered SRAM before a destructive system reset will become active.
 4.60V: When the power drops below this voltage level, a system reset will be released and lasts until the voltage has risen over 4.80V again. An active system reset disables the access to the SRAM.

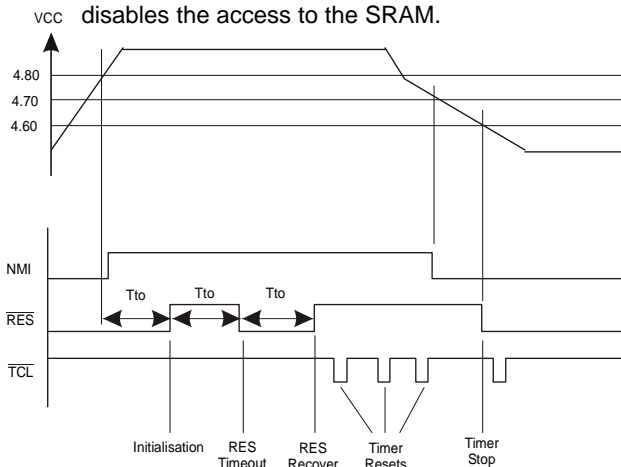


Fig. 3.3.2 Watchdog timing and powerfail reaction

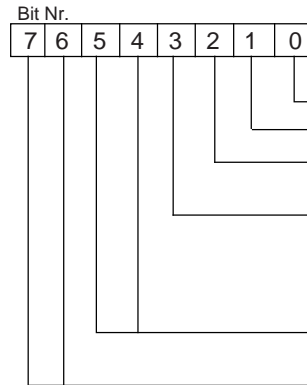
For more information about watchdog and powerfail, see data sheet H6060 from EM Microelectronic-Marin.

3.3.3 SERIAL INTERFACE & SPECIAL PORTS (U32)

The Dual Universal Asynchronous Receiver/Transmitter 68C681 is used for the serial interface. It consists of two serial channels with independent programmable baud rate from 50 to 38400 Baud. Each channel can be used as a 5-wire communication interface (TxD, RxD, RTS, CTS and GND). The vectored interrupt and the 16 Bit counter/timer are two additional features. The DUART is clocked with a 3.6864 MHz crystal oscillator.

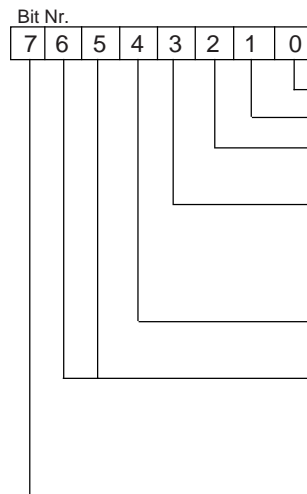
Besides these features there is an 8-bit Output Port and a 6-bit Input Port which can be used as multipurpose I/Os. Some of these port-bits are used for serial communication, some have special functions within the MPL 4080B. Both ports are described below.

Input Port:



- IP0: CTS Channel A
- IP1: CTS Channel B
- IP2: Data In of serial EEPROM
- IP3: IRQ-State (= Flag) of SIMM Module
- 0: IRQ active
- 1: IRQ inactive
- IP4-IP5: Read 2-Bit configuration set at J19
- IP6-IP7: No function

Output Port:



- OP0: RTS Channel A
- OP1: RTS Channel B
- OP2: CLK for the serial EEPROM
- OP3: ChipSelect for the serial EEPROM
- 0: CS active
- 1: CS inactive
- OP4: Data Out for serial EEPROM
- OP5-OP6: Controls the optional LED's
- 0 = on
- 1 = off
- OP7: Memory bank 0 switch (EPROM fade in, see 3.1.1)
- 0: regular function
- 1: state after reset

All output port bits are "1" after reset. See the data sheet from Motorola (MC68681), EXAR (XR-68C681) or Philips (SCC68692) for a detailed description of the DUART.

3.3.4 PARALLEL INTERFACE & TIMERS (U29,U30)

The devices used for the parallel interface are two VIA 65SC22. VIA 1 is located at U29 and VIA2 at U30. These devices offer different modes of operation. In total four parallel ports (8 bits each) with handshake signals (2 each) are provided. The 4 timers can be used for time-slice generation in a real-time operating system, to count pulses, and generate frequencies.

See the data sheet from CMD (Califonia Micro Devices, 65SC22) or from Rockwell International (65NC22) for a detailed description.

Note:

The I/O's of both VIAs are directly connected to connector J3. There are no additional drivers provided. For some applications (i.e. centronics interface), external driving of the I/O's might be necessary.

3.3.5 SERIAL EEPROM (U33)

The mounted 3-wire serial EEPROM (location U33, part number 93C46) is a 1024 bit memory device, organized in 64 registers of 16 bits each.

The serial EEPROM can be programmed, read or written via the DUART ports (see 3.3.3). The ChipSelect (CS, active high) is inverted since the DUART output OP3 is high after reset. Fig. 3.3.5 illustrates the interconnection DUART <—> serial EEPROM.

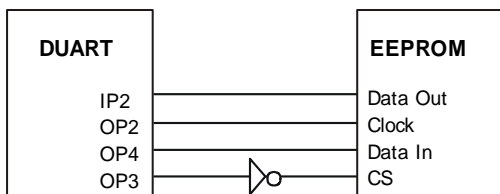


Fig. 3.3.5 Interconnection DUART- EEPROM

Important Note:

Comparing EEPROM devices with the part number '93C46' shows differences in the programming sequence: Some devices do not need an Erase and/or Erase All instruction prior to a Write and/or Write All instruction since they erase automatically on Write/Write All instructions. MPL cannot guarantee to generally equip the MPL 4080B either with devices with or without automatic erase feature. Therefore, the 3-wire serial EEPROMs equipped on the MPL 4080B require an Erase and Erase All cycle prior to the Write and Write All instruction! Some of the manufactures listed below offer devices with automatic erase feature. However, they all have to be pro-

grammed the conservative way. The following data sheets can be consulted: Samsung (KM93C46), Hyundai (HY93C46), SGS-Thomson (ST93C46A), Catalyst Semiconductor (CAT93C46), OKI (MSM16811RS), Atmel (AT93C46), National Semiconductor (NMC93C46).

3.3.6 REAL TIME CLOCK (U36)

The real time clock is the RTC72423 from Seiko. The circuit is clocked with an integrated 32'768 Hz crystal oscillator and offers time and date functions. Only the lower four data bits are used and connected.

For more information see the data sheet RTC72423 from Seiko (or the data sheet of RTC72421 which is the DIL-version of the functionally identical chip).

Note:

The STD.P-output (pin 1) is not used.

3.3.7 CONFIGURATION PORT

The MPL 4080B provides a special 4-bit port. This configuration port reflects the state of the user selectable jumper configuration at J17 (see 2.3.14).

3.4 G-64/96 BUS DESCRIPTION

3.4.1 G-64/96 BUS INTERFACE

The bus interface of the MPL 4080B represents a full support of the G-96 (and G-64) bus. Synchronous and asynchronous 8/16 Bit peripherals in the predecoded VPA-range (1 kWord) and up to 12 MByte in the asynchronous VMA-range can be addressed. Two vectored and three auto-vectored interrupts are supported.

All bus drivers are of 48mA-type and meet the specifications of a hard-terminated G-64/96 backplane (330/470 Ohm networks at each end of the backplane). Table 3.4.1 shows the signals provided on the G-96 bus connector:

Signal	Type (1)	Description	Comment
D0 - D15	I/O	Data lines	
A0 - A23	OUT	Address lines	
/VPA	OUT	Valid peripheral signal	predecoded with A23..A16 and A10
/VMA	OUT	Valid memory address	valid for addresses \$400000
/DS0, /DS1	OUT	Data strobes	valid during /VPA- and /VMA-cycles
R/W	OUT	Read/write signal	
/BRQ, /BGACK	IN	Bus arbitration signals	see 3.4.2 for more information
/BG	OUT	Bus arbitration signal	see 3.4.2 for more information
/IRQ1 - 3, /IRQ5, /NMI	IN	Interrupt lines	
/RES	OC OUT (2)	Reset	
E	OUT (3)	CPU Enable	1/10 of CPU clock
SYCLK	OUT (4)	System clock	1/1 of CPU clock
/IACK	OUT (3)	Interrupt acknowledge	used for vectored levels 3 and 5
/BERR	IN	Bus error	wired-and with the on-board BERR
/HALT	IN	CPU halt	all G-96 outputs go high impedance
/DTACK	IN	Data acknowledge	for asynchronous data transfer
/PWF	IN (5)	Powerfail	wired-and with the on-board PWF
/Page	OUT	Memory expansion	connected to CPU address line A17
CHOUT	Passive	Daisy chain out	pulled up to +5V (3k3)

Table 3.4.1 G-96 bus signal description

Notes:

- (1) Seen from the MPL 4080B
- (2) RESET is an open collector output but NOT bidirectional.
- (3) Enable and IACK are tri-state outputs (high impedance during bus arbitration or HALT).
- (4) SYCLK is a copy of the CPU clock and a tri-state output (high impedance during bus arbitration or HALT).
- (5) In older G-64 bus designs (prior to 1984), pin 29a is a -5V INPUT and has to be open. Since then, pin 29a has changed its function and has now become a Power Fail input and is supported by the MPL 4080B (level 7 interrupt).

For more details refer to the G-64/G-96 SPECIFICATIONS MANUAL Rev.3.

3.4.2 BUS ARBITRATION

The MPL 4080B offers bus arbitration capability. Three control signals are dedicated to that purpose: /BRQ, /BG and /BGACK. If a device requests the G-96 bus, the bus arbitration timing of Fig. 3.4.2 has to be met. For a correct timing, the bus requesting device must monitor several signals, i.e. VMA, VPA and DTACK have to be negated before the bus requesting device is allowed to release the /BGACK signal.

Nr.	Description	Min [ns]	Max [ns]
1	/BRQ low to /BG low	100	480
2	/BGACK active to bus high-Z		40
3	/BGACK low to /BRQ high	20	80
4	/BRQ high to /BG high		480
5	/BGACK low width	200	

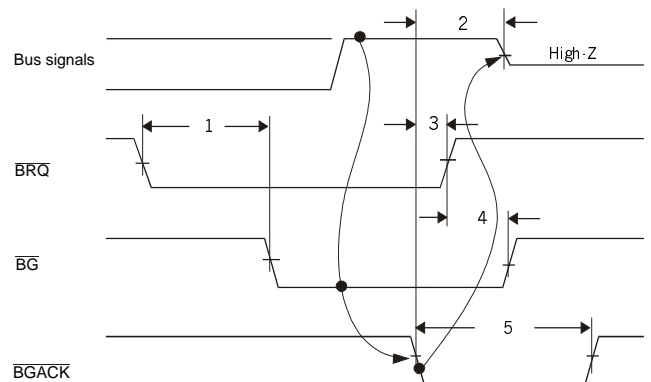


Fig. 3.4.2 Bus arbitration timing

4. MLX LOCAL EXTENSION BUS

The MPL 4080B can be customized through the use of its local extension bus. Although the notion of a local bus is now very common in the industry, the board's Mpl Local eXtension bus (MLX) is designed to allow the easy addition of very simple and very low cost peripheral devices. A selection of MLX add-on modules is already available and others may be custom designed by MPL AG or the user, in order to adapt the MPL 4080B to a specific requirement.

4.1 SIGNAL DESCRIPTION AND PIN ASSIGNMENT

The MLX bus uses a 0.1 inch centerline, single row 30-pin MICRO-EDGE SIMM connector from AMP. Signal description and pin assignment are shown in table 4.1

Pin Number	Signal	Type	Description
1	VCC	PWR	+5V power
2	GND	PWR	Ground
3	D0	I/O	Data line
4	D1	I/O	Data line
5	D2	I/O	Data line
6	D3	I/O	Data line
7	D4	I/O	Data line
8	D5	I/O	Data line
9	D6	I/O	Data line
10	D7	I/O	Data line
11	A1	IN	Address line
12	A2	IN	Address line
13	A3	IN	Address line
14	A4	IN	Address line
15	/CS-MOD	IN	Module Select
16	E	IN	Enable signal
17	R/W	IN	Read/Write control
18	/RES	IN	Reset
19	/IRQ	OC OUT(1)	Interrupt
20	GND	PWR	Ground
21	SIMM0	I/O	Multi-purpose I/O(2)
22	SIMM1	I/O	Multi-purpose I/O(2)
23	SIMM2	I/O	Multi-purpose I/O
24	SIMM3	I/O	Multi-purpose I/O
25	SIMM4	I/O	Multi-purpose I/O
26	SIMM5	I/O	Multi-purpose I/O
27	SIMM6	I/O	Multi-purpose I/O
28	SIMM7	I/O	Multi-purpose I/O
29	SIMM8	I/O	Multi-purpose I/O
30	SIMM9	I/O	Multi-purpose I/O

Table 4.1 MLX bus pin assignment

Notes:

- (1) open collector output signal
- (2) Signals SIMM0 and SIMM1 are not connected on the MPL 4080B and cannot be used as I/Os. Signals SIMM2-SIMM9 are wired to connector J3.

4.2 SIGNAL TIMING

The MLX bus supports only synchronous cycles. The timing specification given in Fig.4.2.B and Table 4.2.A assumes that synchronous peripheral devices will be used on the module. Table 4.2.A shows two columns. The first shows the minimum times when using 1 MHz peripheral devices (68000 with 8 MHz), the second shows the corresponding timings when using 2 MHz peripheral devices (68000 with 16 MHz).

Timing	Description	Speed of peripheral device	
		1MHz Min.(ns)	2MHZ Min.(ns)
1	Enable pulse width high	450	220
2	Address lead time	220	100
3	Address hold time	20	20
4	ChipSelect lead time	170	70
5	ChipSelect hold time	20	10
6	Write control lead time	220	100
7	Write control hold time	20	20
8	Data setup time write	430	200
9	Data hold time write	30	10
10	Data setup time read	80	50
11	Data hold time read	10	10

Table 4.2.A MLX bus timing information

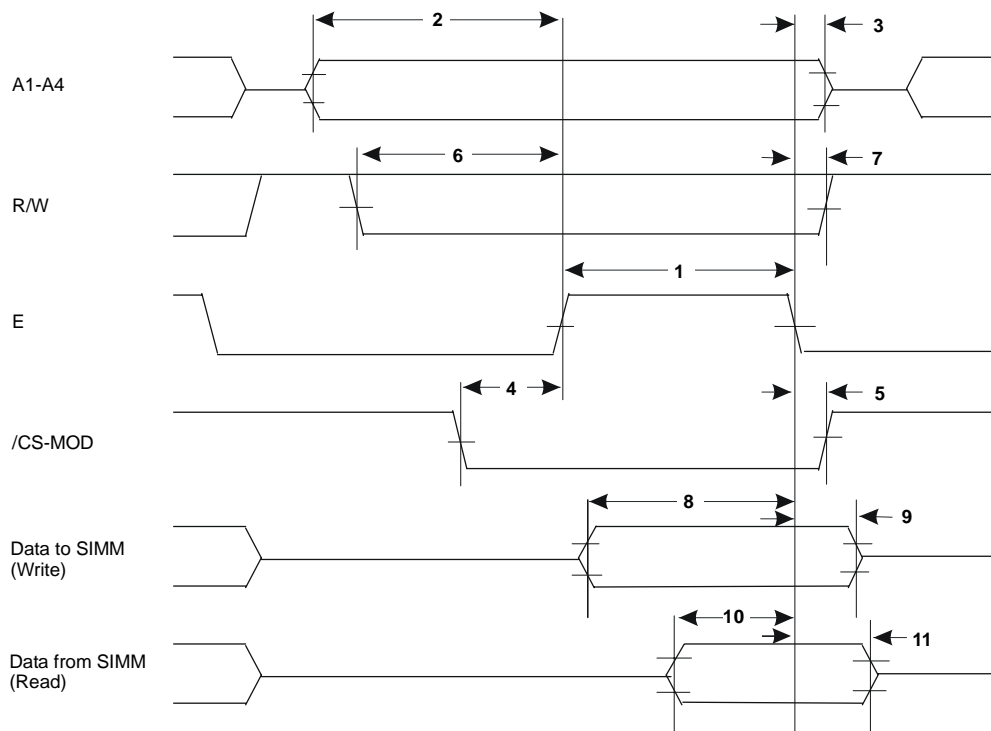
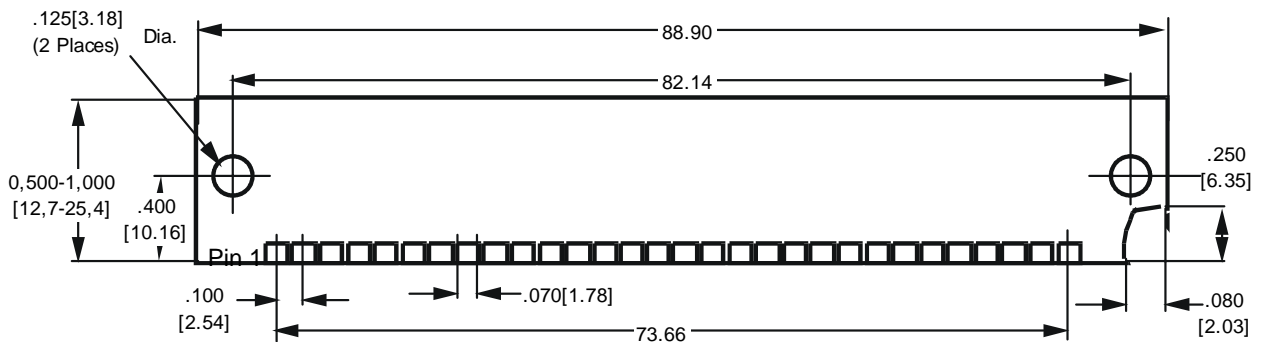


Fig. 4.2.B MLX bus timing diagram

4.3 MLX BUS MECHANICAL DIMENSIONS

Figure 4.3 shows the typical dimensions of a MLX expansion module.



Thickness of PCB: 1.19 to 1.37mm

Fig 4.3 MLX bus module mechanical dimensions

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This manual reflects the Rev. B of the MPL 4080B

Publication Date : January 1993

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Disregarding my wish will not break the license agreement or any other contracts. However, ignoring it would mean not respecting the thoughts I had when putting my efforts into this product.

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