

## MPL INDUSTRIAL PC WITH AMD Élan™SC520 PROCESSOR (5x86)

The MIP520 is a highly integrated industrial single board computer in PC/104 form factor. It is fully PC/AT compatible and well suited for applications requiring a small size, high performance PC with great flexibility. The MIP520 can be used in a standard operating environment without the necessity of a fan.

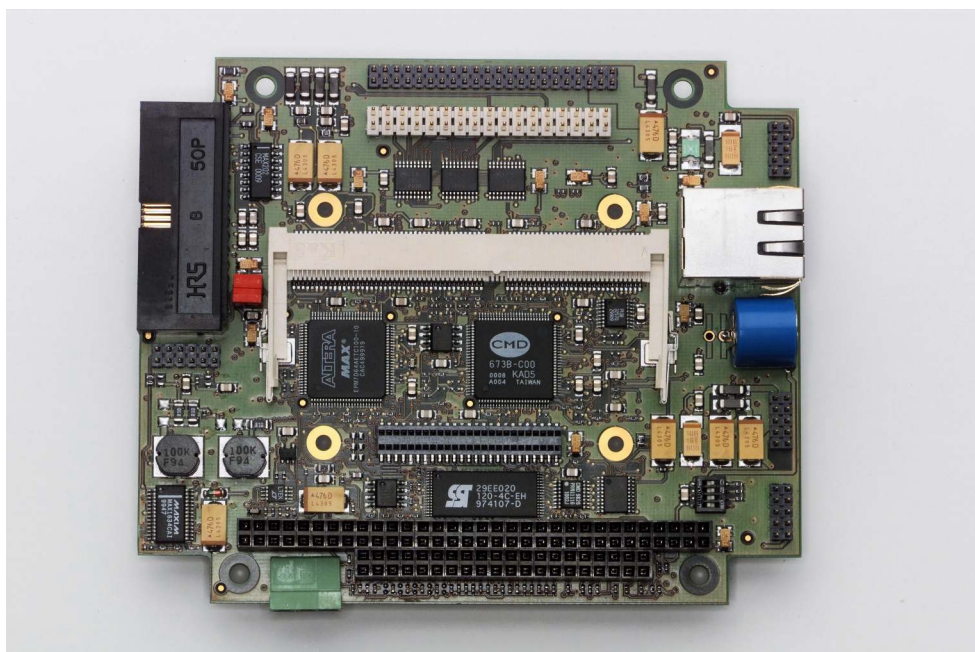
All major components required to build a complete and sophisticated PC/AT system are implemented on a single PC/104 sized board. It features a graphic interface for flat panel and CRT (simultaneous panel and CRT operation possible), an E-IDE and a FDD port, one parallel and four serial ports, keyboard and mouse interface, SSI, speaker output, timer interface and a real time clock. Also an ethernet and/or an USB controller are on board. The 16-bit PC/104 interface offers easy and flexible expansion capabilities.

Integration of the MIP520 into a system is facilitated by the fact of offering standard connectors for FDD (34 pin header), E-IDE (44 pin header) and LAN (RJ45). The serial and parallel interfaces can be accessed through a standard 1.27mm flat ribbon cable offering the ability for a one to one connection to standard IDC type DSUB connectors. Keyboard and mouse are also accessible through a 1.27mm flat ribbon cable. All other signal connections are established by 2mm pin headers. Particular precaution has been taken to the EMC so that an entire system can fulfill the CE and FCC requirements.

All these features make the MIP520 to the ideal solution for any low-cost embedded control application where a flexible and fully compatible PC/AT is needed.

### Features

- AMD Élan™SC520 Processor @ 133MHz
- 144-pin SO-DIMM socket for SDRAM
- Flash BIOS ROM
- RTC and Setup with battery backup
- Programmable watchdog
- PC/104 interface
- Integrated graphic controller with CRT and Panel Support
- E-IDE & FDD standard ports
- Two RS232 serial & one parallel port
- Two additional TTL serial ports
- PS/2 keyboard & mouse interface
- SSI and Timer interfaces
- Speaker interface
- Two USB ports
- Integrated 10/100 Mbit/s Ethernet Controller with RJ45 connector



MIP520-1 Rev.A

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## 1. INTRODUCTION

### 1.1 ABOUT THIS MANUAL

This manual assists the installation and initialization procedure by providing all the information necessary to handle and configure the MIP520.

The manual is written for technical personnel responsible for integrating the MIP520 into their system.

### 1.2 SAFETY PRECAUTIONS AND HANDLING

For personal safety and safe operation of the MIP520, follow all safety procedures described here and in other sections of the manual.

- Power must be removed from the system before installing (or removing) the MIP520 to prevent the possibility of personal injury (electrical shock) and/or damage to the product.
- Handle the product carefully, i.e. dropping or mishandling the MIP520 can cause damage to assemblies and components.
- Do not expose the equipment to moisture.

#### WARNING

**There are no user-serviceable components on the MIP520**

### 1.3 ELECTROSTATIC DISCHARGE (ESD) PROTECTION

Various electrical components within the product are sensitive to static and electrostatic discharge (ESD). Even a non-sensible static discharge can be sufficient to destroy or degrade a component's operation!

Following the precautions listed below will avoid ESD-related problems:

- Use a properly installed anti static pad on your work surface.
- Wear wrist straps and observe proper ESD grounding techniques.
- Leave the unit in its anti static cover until you are prepared to install it in the desired environment. When it is out of its protection cover, place the unit on the properly grounded anti static work surface pad.
- Do not touch any components on the product. Handle the product by its card edges.

### 1.4 EQUIPMENT SAFETY

Great care is taken by MPL that all its products are thoroughly and rigorously tested before leaving the factory to ensure that they are fully operational and conform to specification. However, no matter how reliable a product, there is always the remote possibility that a defect may occur. The occurrence of a defect on this device may, under certain conditions, cause a defect to occur in adjoining and/or connected equipment. It is the user's responsibility to ensure that adequate protection for such equipment is incorporated when installing this device. MPL accepts no responsibility whatsoever for such kind of defects, however caused.

## 2. GENERAL INFORMATION AND SPECIFICATIONS

This section provides a general overview over the MIP520 and its features. It outlines the electrical and physical specifications of the product and its power requirements.

### 2.1 PRODUCT DESCRIPTION

#### AMD Élan™ SC520-133MHz CPU

The Élan™ SC520 microcontroller combines a 32-bit, low-voltage Am5x86 CPU with a complete set of integrated peripherals suitable for both real-time and PC/AT-compatible embedded applications. It has a 16-Kbyte write-back or write-through cache, Floating Point Unit (FPU), Integrated PC/AT peripherals and a Synchronous Serial Interface (SSI). The device also features a 32-bit PCI bus, a high-performance, 32-bit SDRAM interface and a full-featured, high-performance incircuit emulation capability, known as the AMDebug™ utility.

The instruction set includes the complete 486 microprocessor instructions and is compatible to every member of the x86 family. Because of the processor operating frequency of 133MHz, system performance increases over a Pentium P75, while maintaining complete compatibility with the standard 486 processor architecture.

#### Memory

The MIP520 is equipped with one standard 144-pin SO-DIMM socket for an SDRAM Module.

#### SDRAM

One SDRAM SO-DIMM module can house up to 256 Mbytes.

#### Storage

External mass storage devices such as hard disks and floppy disks can be connected to the E-IDE and FDD interfaces. The local-bus E-IDE interface supports all ANSI standard devices using PIO modes 0,1 and 2 (two devices in master/slave configuration are supported). The FDD port allows operation with one or two floppy disk drives up to 2.88 Mbytes.

#### 16-bit PC/104 interface

The MIP520 is a true single board computer with all PC/AT features on board and therefore the use of a backplane is not required. Nevertheless the standard PC/104 interface allows flexible extension with additional peripherals (stacked on the PC/104 connector).

#### Software

The MIP520 is set up with the General Software BIOS. Any operating system for a PC/AT can be run on the MIP520.

#### Industrial Quality

The MIP520 provides all aspects of quality demanded of an industrial computer system. Development according to EMC requirements supports the user in achieving the CE conformity on the system level. This covers features like on board protection/filter devices on power and I/O lines as well as a carefully designed layout.

#### Applications

Data acquisition and Industrial control  
Measurement equipment  
Single board concepts (Thin clients, Web browsers PC Peripherals, etc.)  
Power critical designs  
Portable microcomputer  
and many more

## 2.2 SPECIFICATIONS

### 2.2.1 ELECTRICAL

#### Processor:

AMD Élan™ SC520:

- Industry-standard Am5x86 CPU
- Floating Point Unit (FPU)
- 32-Bit data bus
- 16 Kbytes write-back or write-through cache
- 100 or 133 MHz operating frequency
- Integrated PCI host bridge controller
- Synchronous DRAM (SDRAM) controller
- Enhanced DMA controller
- Enhanced programmable interrupt controller (PIC)
- Programmable interval timer (PIT)
- Real-time clock (RTC)

#### Super IO:

- Floppy disk controller
- PS/2 Keyboard and Mouse controller
- IEEE1248 compliant parallel port (ECP/EPP)
- Two serial ports, optional Fast Infrared Interface on UART2
- ISA host interface

#### Graphic:

- 64 bit graphic engine
- 2 Mbytes video memory
- Resolutions up to 1280x1024 pixels
- Colors up to 64k
- Refresh-rates up to 85 Hz
- DPMS and DDC support
- Simultaneous CRT and panel operation
- MPL REMMI-T (PanelLink™ transmitter) module port, flexible panel support for STN and TFT panels, resolutions up to 1280x1024

#### BIOS ROM:

- 256kB Flash EEPROM (256k x 8; 128 Bytes per page, 2048 pages)
- easy BIOS update

#### Memory:

- Socket for one 144 pin SO-DIMM memory module with 4k refresh
- 3.3V<sub>DC</sub> 66 MHz SDRAM or faster can be used
- Supports 16-, 64-, 128- and 256Mbit SDRAM technology
- Up to 256 Mbytes (1 module)
- 64-bit data bus
- Error Correction Code (ECC) is not supported

#### RTC and CMOS Setup:

- RTC backed with on board battery

**PC/104 interface:**

- 16 Bit PC/104 interface
- External bus master not supported
- The MIP520 is a stackthrough 16-bit module

**Serial RS232 ports:**

- Two serial RS232 ports, COM1 and COM3
- 16C550 compatible (16Byte FIFOs)
- Flexible interrupt setting features for the ports
- COM1 with all modem signals except DCD
- COM3 full modem signal interface
- Both ports are ESD protected
- Available on 50-pin connector

**Serial TTL ports:**

- Two serial TTL ports, COM2 and COM4
- 16C550 compatible (16Byte FIFOs)
- Flexible interrupt setting features for the ports
- COM2 with RxD, TxD and all handshake signals
- COM4 only RxD and TxD are available
- Optionally COM4 can be used as Infrared Interface port
- Available on 12-pin header, 2mm pitch

**Parallel port:**

- One IEEE1284 compliant port
- SPP, EPP1.7, EPP1.9, ECP mode support
- Configurable as LPT1, LPT2, LPT3
- ESD protected
- Available on 50-pin connector

**Keyboard / Mouse:**

- Serial PS/2 interfaces
- ESD protected
- Available on 50-pin connector

**E-IDE port:**

- One port for up to two drives
- ANSI Standard modes 0, 1 and 2
- Available on 44-pin header, 2 mm pitch

**Floppy disk:**

- One port for up to two drives
- Up to 2.88 Mbytes FDD supported
- Available on 34-pin standard header, 2.54 mm pitch

**SSI, Timer and Speaker:**

- No ESD protection
- Available on 10-pin header, 2mm pitch

**Miscellaneous:**

- Connection for an external remote reset switch
- Software timer provide a millisecond timebase with microsecond resolution (max. 65.5sec)
- Programmable watchdog timer with distinct keyed write sequence (timeout duration configurable between 0.5msec .. 32sec)

**USB:**

- PCI to USB host controller
- Full 32-bit PCI bus master
- Two USB 1.1 ports for serial transfers up to 12 Mbit/s
- USB keyboard/mouse is supported by the BIOS
- ESD protected
- Available on 10-pin header, 2mm pitch

**Ethernet:**

- Fast 10/100 Mbps PCI to ethernet controller
- Full 32-bit PCI bus master
- 10Base-T/100BaseTX interface (IEEE 802.3), supports Auto-Negotiation
- Activity Indicators for network traffic and 100 Mbps operation on connector
- Device drivers for all major operation systems available
- ESD protected
- Available on RJ45 connector

## 2.2.2 PHYSICAL/POWER

**Form factor:**

PC/104, with connectors in defined I/O connectors overhang regions

Length: 95.9 mm (3.775 inches)

Width: 115.6 mm (4.550 inches)

Height: 14.0 mm (0.550 inch) (excluding PC/104 bus connectors)

**Weight:**

Typical 110g (fully equipped, without memory module)

**Power supply:**

Over PC/104 bus interface or through separate 3-pin Mini-Combicon power connector.

**Input Power requirement:**

+5V: +5VDC  $\pm$  5%

**Power consumption:**

Typ. 800mA@5V (with Ethernet, USB and 64MB SDRAM, without panel)

## 2.2.3 ENVIRONMENT

**Temperature range:**

0°C to +60°C (+32°F to +140°F) @ 133 MHz CPU speed without heat sink

extended temperature range available

**Relative humidity:**

10% ... 90% non condensing

### 2.3 DIMENSIONS

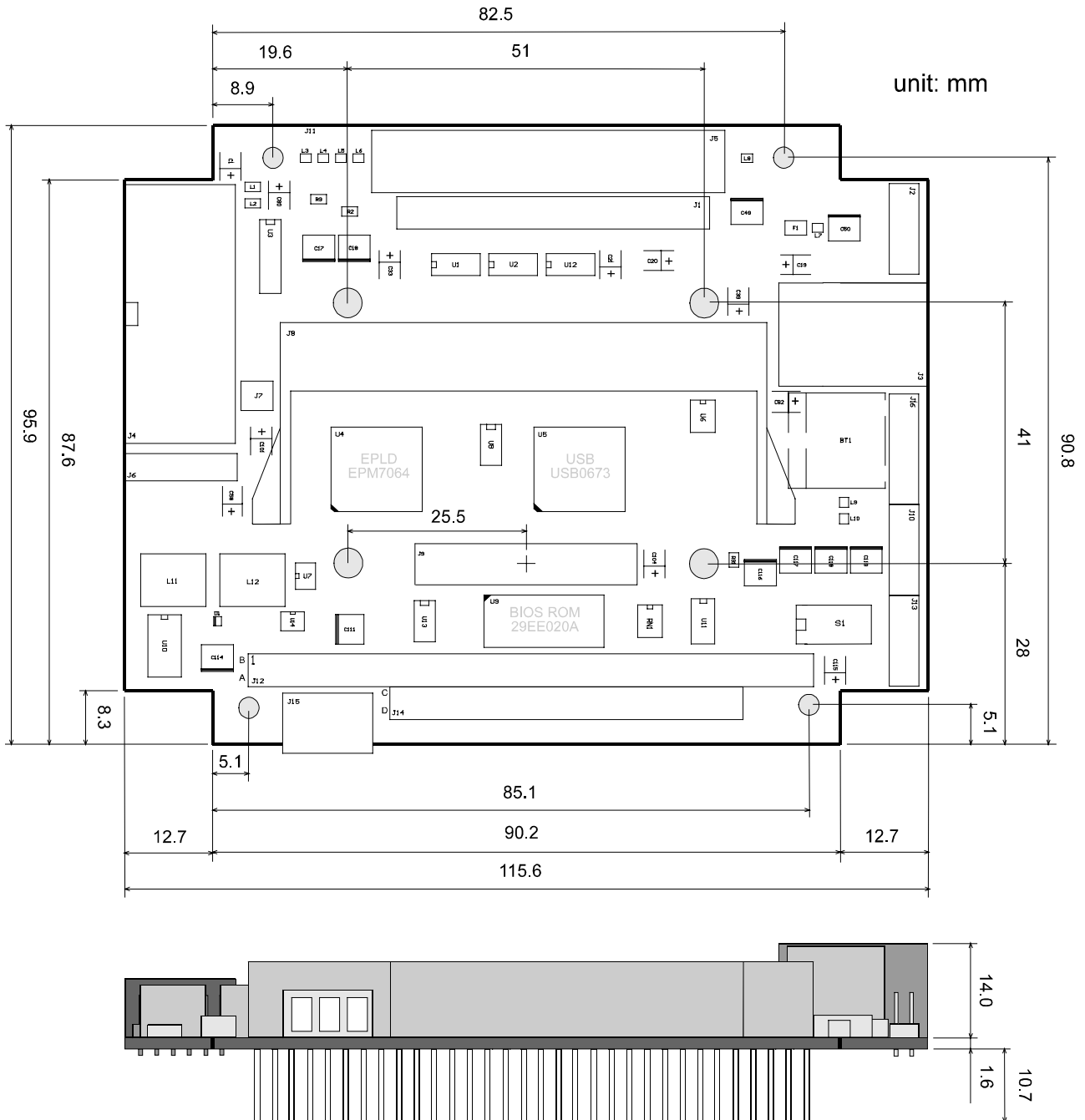


Figure 2-1 Dimensions MIP520

## 2.4 DIFFERENCES TO PREVIOUS REVISIONS

Between the former MIP520 revisions A to C and revision D, or above, some major changes have been made. This changes are mainly because of the new available Élan™SC520 with Mask B0. This also means, that this manual can not be used for the former MIP520 revisions.

This section is thought particularly for users of devices of the former revisions and shall show the differences which are important at exchange, etc. Please contact your local distributor or MPL AG for further information about the changes.

### 2.4.1 CHANGES

- New Élan™SC520 Mask B0 mounted on board – now 4 serial ports available
- New pinout of connectors J4 and J16 – due to the new serial ports
- 32.768 kHz quartz mounted instead of an oscillator – leads to longer battery lifetime
- Stronger pull up resistors on PC104 datalines – leads to faster switch back times

### 3. PREPARATION FOR USE

#### 3.1 PARTS LOCATION

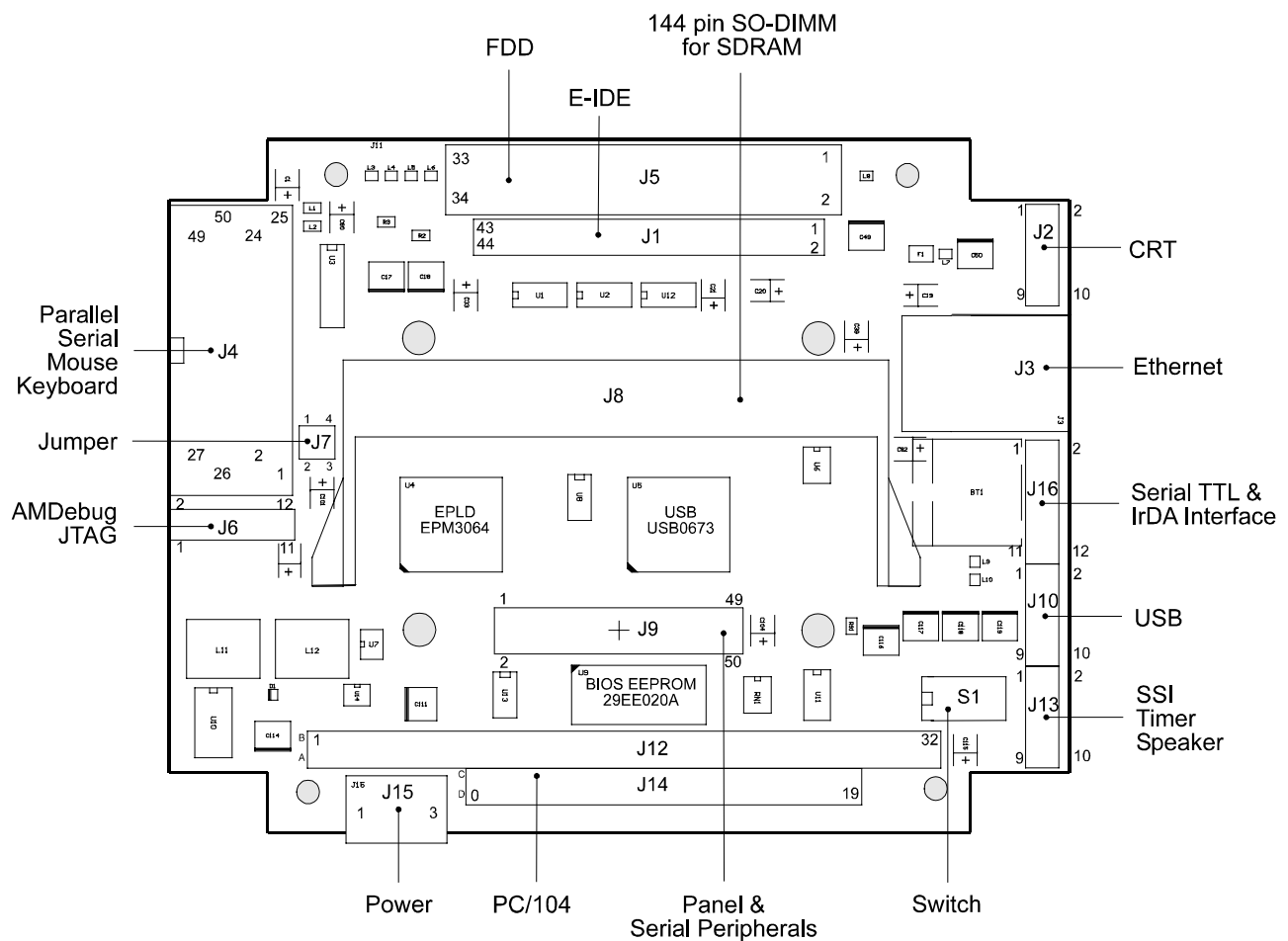
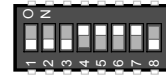


Figure 3-1 Parts Location

### 3.2 SWITCH AND HARDWARE SETTINGS



#### 3.2.1 DIP SWITCH 1 – AMDebug options, Display settings & Battery backup

This DIP switch is for are user settable configuration options. The default switch settings are in brackets.

Switch S1					Meaning
SW1-1	ON				Serial Console on (Kb & VGA to COM1)
	(OFF)				Serial Console off
SW1-2	ON				AMDebug Enter is turned on
	(OFF)				AMDebug Enter is turned off
SW1-3	ON				AMDebug Instruction Trace is turned on
	(OFF)				AMDebug Instruction Trace is turned off
SW1-4...7 (Note 1)	(ON)	(ON)	(ON)	(ON)	TFT Panel with 640x480 (VGA)
	OFF	ON	ON	ON	TFT Panel with 800x600 (SVGA)
	ON	OFF	ON	ON	TFT Panel with 1024x768 (XGA)
	OFF	OFF	ON	ON	TFT Panel with 1280x1024 (SXGA)
	ON	ON	OFF	ON	TFT Panel with 320x240 (QVGA)
	OFF	ON	OFF	ON	Panel Type #5 (TBD)
	ON	OFF	OFF	ON	Panel Type #6 (TBD)
	OFF	OFF	OFF	ON	Panel Type #7 (TBD)
	ON	ON	ON	OFF	Panel Type #8 (TBD)
	OFF	ON	ON	OFF	Panel Type #9 (TBD)
	ON	OFF	ON	OFF	Panel Type #10 (TBD)
	OFF	OFF	ON	OFF	Panel Type #11 (TBD)
	ON	ON	OFF	OFF	Panel Type #12 (TBD)
	OFF	ON	OFF	OFF	Panel Type #13 (TBD)
	ON	OFF	OFF	OFF	Panel Type #14 (TBD)
SW1-8	ON				Battery backup on
	(OFF)				Battery backup off

**Table 3-1 DIP Switch 1**

Note:

1. Panel Types are to be defined. Please contact your distributor or MPL AG for further information.

#### 3.2.2 Hardwired USB PORT1 Routing

The USB datasignals of port1 can be routed either to the USB connector (J10) or to the Panel & serial Peripherals connector (J9). This is done by an assembly option, per default the signals are routed to the USB connector (please ask MPL AG for detailed information).

### 3.3 MEMORY MODULE SOCKET

#### 3.3.1 SDRAM MEMORY MODULE

A 144-pin SO-DIMM socket with JEDEC standard layout is available for system memory. The Serial Presence Detect (SPD) feature and Error Correction Code (ECC) are not supported on the MIP520. Single or double sided memory modules may be inserted. The SDRAM Controller of the MIP520 supports up to 256 Mbytes of SDRAM. The timing of the SDRAM interface can be adjusted by using the registers in the Élan™ SC520 (usually established by BIOS setup).

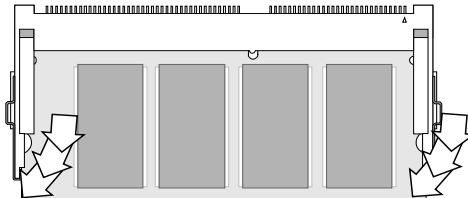
For better air circulation it is recommended to use a single side memory module (1 bank). The MIP520 accepts only SDRAM modules with the following specification!

#### Electrical and mechanical requirements for the SO-DIMM Memory Module:

- 3.3V type
- Speed 15ns or faster (66MHz; PC66 compliant)
- SDRAM devices with 16-, 64-, 128- or 256-Mbit density, 8 through 11 column address bits and 11 or 12 row address bits (4k Refresh)
- Gold contacts (tin contacts would also work but are not recommended)
- JEDEC Standard SO-DIMM 144-Pin layout
- The memory module can be maximum 28mm wide (JEDEC standard is 25.4mm)

#### 3.3.2 MOUNTING THE MEMORY MODULE

Please insert the Memory Module very carefully! Please pay attention to correct alignment of the modules keys and do not apply excessive force.



**Figure 3-2 Mounting the memory module**

### 3.4 CONNECTORS

#### 3.4.1 PARALLEL, SERIAL, MOUSE, KEYBOARD CONNECTOR (J4)

J4 is a 50-pin HIROSE high density connector (male) with the signals for a parallel port, a mouse port, a keyboard port and two RS232 ports. COM3 is a full modem interface located on pins 26 to 34. COM1 has all signals except DCD and is on pins 35 to 42.

The pinout of this connector is designed for a 1:1 wiring with flat ribbon cables to standard IDC DB25 (parallel port) and DB9 (serial ports) connectors, see section 3.5.

50-pin HIROSE MINI-FLEX connector HIF6A-50PA-1.27DS pinout:

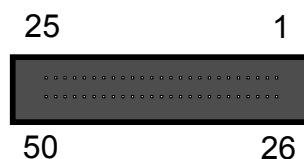
Pin number	Signal	Pin number	Signal
1	/Strobe	26	GND
2	/Auto Line Feed	27	RI3
3	Data0	28	DTR3
4	/Error	29	CTS3
5	Data1	30	TXD3
6	/Init	31	RTS3
7	Data2	32	RXD3
8	/Select In	33	DSR3
9	Data3	34	DCD3
10	GND	35	GND (Note 1)
11	Data4	36	RI1 (Note 1)
12	GND	37	DTR1 (Note 1)
13	Data5	38	CTS1 (Note 1)
14	GND	39	TXD1 (Note 1)
15	Data6	40	RTS1 (Note 1)
16	GND	41	RXD1 (Note 1)
17	Data7	42	DSR1 (Note 1)
18	GND	43	MSDAT
19	/Acknowledge	44	MSCLK
20	GND	45	VCC
21	Busy	46	GND
22	GND	47	KBDAT
23	Paper End	48	KBCLK
24	GND	49	VCC
25	Select	50	GND

**Table 3-2 Parallel-, Serial-, Mouse, Keyboard port**

Note:

1. These assignments are true from production revision D on (see section 7.3).

Pin numbering of on board 50pol HIF6A-50PA-1.27DS connector:



Counterpart is the HIROSE MINI-FLEX connector HIF6-50D-1.27R. For easy connection see section 3.5 .

**3.4.1.1 USING THE PARALLEL PORT AS FLOPPY DISK PORT**

The parallel port can also operate as external Floppy Disk Port. The two modes can be switched in the BIOS setup ("Custom Configuration"). See Table 3-3 for the corresponding pin configurations if parallel port is used as floppy disk port.


Floppy Disk Mode on parallel Port		
Pin number J4	Signal	Description
1	DS0	Drive Select 0
2	IDX	Index
3	TR00	Track 0
4	WP	Write protected
5	RDATA	Read Data
6	DSKCHG	Disk Change
7	MID0	Media ID 0
8	MTR0	Motor On 0
9	MID1	Media ID 1
10	DS1	Drive Select 1
11	MTR1	Motor On 1
12	WDATA	Write Data
13	WGATE	Write Gate
14	DRVDEN0	Drive Density 0
15	HDSEL	Head Select
16	DIR	Direction
17	STEP	Step
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground
25	GND	Ground

**Table 3-3 Parallel port on 50pol connector used as Floppy Disk Port**

### 3.4.2 POWER CONNECTOR (J15)

This connector is needed if no power via PC104 bus is provided. No other inputs than this and the power inputs on PC104 bus must be used to power the board.

3-pin power connector Phoenix Contact AG typ MC1,5/3-G-3.81 pinout:

Pin number	Signal	Description	Pinout
1	$V_{IN}$	Input voltage (+5 V <sub>DC</sub> )	
2	GND	Ground	
3	SRESET#	System Reset Input (active low)	

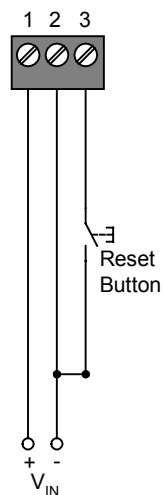
**Table 3-4 Power connector**

Counterpart is the Phoenix Contact AG connector typ MC1,5/3-ST-3.81 (5-10A).

**WARNING**  
**Be aware of the input voltage polarization !**  
**Wrong polarization of the input voltage can cause serious damage to the MIP520 and attached peripherals!**

#### 3.4.2.1 MOUNTING AN EXTERNAL RESET SWITCH

On the SRESET# input on the External Power Connector exists the possibility to mount an external Reset Switch for system reset, see Figure 3-3. The SRESET# input is active low and can be connected directly to an open drain output (internal 10k $\Omega$  pull up resistor to 3.3V).



**Figure 3-3 Mounting an External Reset Switch**

**WARNING**  
**Do not apply other voltages than  $V_{in}$ - or tristate to the SRESET# input!**  
**Exceeding these limits can cause serious damage to the MIP520!**

### 3.4.3 E-IDE CONNECTOR (J1)

There is a standard connector for 2,5" hard disks (44 pin header / 2mm pitch).

44-pin E-IDE pinout:

Pin	Signal	Description	Pin	Signal	Description
1	/RESET	Reset	23	/IOW	I/O write strobe
2	GND	Ground	24	GND	Ground
3	D7	Data bit 7	25	/IOR	I/O read strobe
4	D8	Data bit 8	26	GND	Ground
5	D6	Data bit 6	27	IORDY	I/O ready
6	D9	Data bit 9	28	CSEL	Cable select
7	D5	Data bit 5	29	/DACK	DMA acknowledge
8	D10	Data bit 10	30	GND	Ground
9	D4	Data bit 4	31	IRQ	Interrupt request
10	D11	Data bit 11	32	/IOCS16	I/O Chip Select 16bit
11	D3	Data bit 3	33	A1	Address 1
12	D12	Data bit 12	34	NC (/PDIAG)	Not connected
13	D2	Data bit 2	35	A0	Address 0
14	D13	Data bit 13	36	A2	Address 2
15	D1	Data bit 1	37	/CS0	Chipselect 0
16	D14	Data bit 14	38	/CS1	Chipselect 1
17	D0	Data bit 0	39	NC (/ACTLED)	Not connected
18	D15	Data bit 15	40	GND	Ground
19	GND	Ground	41	VCC Logic	+5VDC Logic
20	KEY	Key / not connected	42	VCC Motor	+5VDC Motor
21	DRQ	DMA request	43	GND	Ground
22	GND	Ground	44	NC	Not connected

**Table 3-5 E-IDE connector**

### 3.4.4 FDD CONNECTOR (J5)

There is a standard connector for floppy disks (34 pin header / 2.54mm pitch).

Standard 34-pin FDD connector pinout:

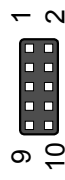
Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	18	/DIR	Step direction
2	DRV DEN0	Drive density 0	19	GND	Ground
3	GND	Ground	20	/STEP	Step pulse
4	NC	Not connected	21	GND	Ground
5	GND	Ground	22	/WDATA	Write data
6	DRV DEN1	Drive density 1	23	GND	Ground
7	GND	Ground	24	/WGATE	Write gate
8	/IDX	Index	25	GND	Ground
9	GND	Ground	26	/TR00	Track0
10	/MTR0	Motor on 0	27	GND	Ground
11	GND	Ground	28	/WPROT	Write protected
12	/DS1	Drive select 1	29	GND	Ground
13	GND	Ground	30	/RDATA	Read data
14	/DS0	Drive select 0	31	GND	Ground
15	GND	Ground	32	/HDSEL	Head select
16	/MTR1	Motor on 1	33	GND	Ground
17	GND	Ground	34	/DSKCHG	Disk change

**Table 3-6 Standard FDD connector**

### 3.4.5 SSI, TIMER & SPEAKER CONNECTOR (J13)

J13 is a 10 pin 2mm pitch header with the signals for SSI-, Timer- and Speaker interface.

10-pin header pinout:

Pin	Signal	Description	Pinout
1	VCC3	+3.3VDC	
2	SSI CLK	SSI Clock	
3	SSI DO	SSI Data Output (data to peripheral)	
4	SSI DI	SSI Data Input (data from peripheral)	
5	SSI EN#	SSI Device Enable (low active)	
6	GND	Ground	
7	TMR1 IN	Timer 1 Input ( $V_{IHmax} = 0.8V$ ; $V_{IHmin} = 2.0V$ ; $V_{Imax} = 5.0V$ )	
8	TMR0 OUT	Timer 0 Output (Totem pole: $V_{OLmax} = 0.5V$ ; $V_{OHmin} = 2.8V$ ; $I_O = 6mA$ )	
9	SPK+ (VCC)	Speaker + (+5V <sub>DC</sub> )	
10	SPK-	Speaker -	

**Table 3-7 SSI, Timer & Speaker connector**

#### 3.4.5.1 SYNCHRONOUS SERIAL INTERFACE (PIN 1 TO 6)

The synchronous serial interface (SSI) provides efficient, bi-directional communication to peripheral devices. The interface can be used to configure and monitor the status of EEPROMs, audio CODECs, DSPs, etc. It can communicate with slave interfaces that are compatible to Motorola's Serial Peripheral Interface (SPI), Serial Communication Port (SCP) and other industry standards.

A complete description of this interface is beyond the scope of this manual. Please refer the documentation of the Élan™SC520 from AMD or/and contact MPL AG for further information and implementation help.

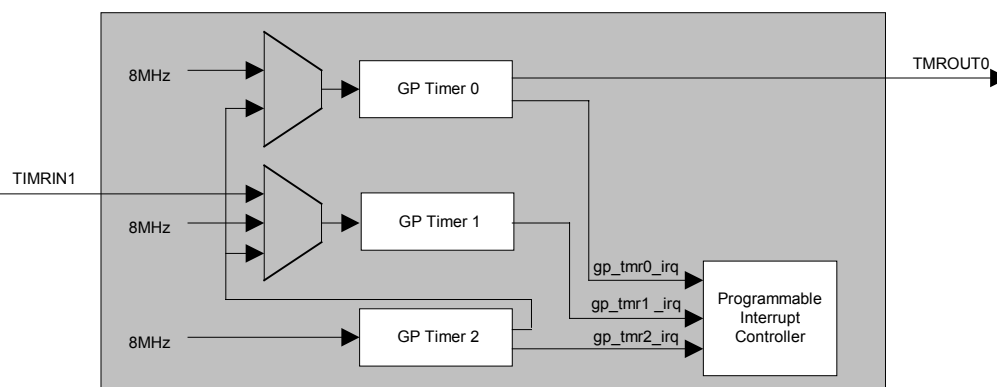
#### 3.4.5.2 TIMER SIGNALS (PIN 7 AND 8)

Timer1 Input can be programmed to be control (for event capture, pulse count) or clock for the general purpose (GP) timer1 in the Élan™SC520. The input frequency range is 0 - 8MHz.

Timer0 Output is the output from the general-purpose timer0 in the Élan™SC520. For example it can be used as pulse-width modulation signal.

Normally the GP-timers are 16-bit timers, but they can be configured as 32-bit timers if necessary.

A complete description of the timer interface is beyond the scope of this manual. Please refer the documentation of the Élan™SC520 from AMD or/and contact MPL AG for further information and implementation help.



**Figure 3-4 General purpose timers on MIP520**

### 3.4.5.3 SPEAKER SIGNALES (PIN 9 AND 10)

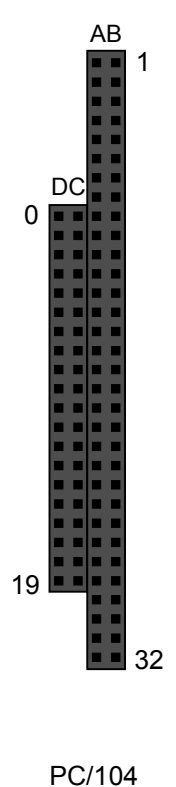
The Speaker– signal is the strengthened Programmable Interval Timer 2 output. It is set up as speaker output by the BIOS. A speaker can directly be connected between SPK- and SPK+ (+5V).

### 3.4.6 PC/104 INTERFACE CONNECTOR (J12/J14)

For system extensions the MIP520 offers a standard 16 bit PC/104 interface. This enables the board to take advantage of the huge selection of peripheral boards in PC/104 form factor currently available.

A complete description of the standard is beyond the scope of this manual. Please refer to the PC/104 Specification, Version 2.3 and to the IEEE P996 draft standard (D2.02) for a more detailed description of the interface.

104-pin standard PC/104 pinout:

Number	Row A	Row B	Row C	Row D	Pinout
0	--	--	GND	GND	
1	/IOCHCK	GND	/SBHE	/MEMCS16	
2	SD7	RSTDRV	LA23	/IOCS16	
3	SD6	+5VDC	LA22	IRQ10 (Note 6)	
4	SD5	IRQ9 *6	LA21	IRQ11 (Note 6)	
5	SD4	(-5V) (Note 1)	LA20	IRQ12 (Note 6)	
6	SD3	DRQ2 (Note 5)	LA19	IRQ15 (Note 6)	
7	SD2	(-12V) (Note 1)		IRQ14 (Note 6)	
8	SD1	/ENDXFR (Note 2)	LA17	/DACK0 (Note 5)	
9	SD0	(+12V) (Note 1)	/MEMR	DRQ0 (Note 5)	
10	IOCHRDY	NC (Key)	/MEMW	/DACK5 (Note 5)	
11	AEN	/SMEMW	SD8	DRQ5 (Note 5)	
12	SA19	/SMEMR	SD9	/DACK6 (Note 5)	
13	SA18	/IOW	SD10	DRQ6 (Note 5)	
14	SA17	/IOR	SD11	/DACK7 (Note 5)	
15	SA16	/DACK3 (Note 5)	SD12	DRQ7 (Note 5)	
16	SA15	DRQ3 (Note 5)	SD13	+5V	
17	SA14	/DACK1 (Note 5)	SD14	/MASTER (Note 2)	
18	SA13	DRQ1 (Note 5)	SD15	GND	
19	SA12	/REFRESH (Note 2)	NC (Key)	GND	
20	SA11	SYSCLK (Note 3)	--	--	
21	SA10	IRQ7 (Note 6)	--	--	
22	SA9	IRQ6 (Note 6)	--	--	
23	SA8	IRQ5 (Note 6)	--	--	
24	SA7	IRQ4 (Note 6)	--	--	
25	SA6	IRQ3 (Note 6)	--	--	
26	SA5	/DACK2 (Note 5)	--	--	
27	SA4	TC	--	--	
28	SA3	BALE	--	--	
29	SA2	+5V	--	--	
30	SA1	OSC (Note 4)	--	--	
31	SA0	GND	--	--	
32	GND	GND	--	--	

**Table 3-8 PC/104 connector**

Notes:

1. Signal not used and not available.
2. Signal is pulled up to +5V<sub>DC</sub>.
3. Standard 8MHz clock.
4. 14.318MHz clock, not synchronized to any other signal.
5. Some DMA channels may be in use of some on board periphery, see section 4.8.
6. Some interrupt channels may be in use of some on board periphery, see section 4.7.

### 3.4.7 PANEL & SERIAL PERIPHERALS CONNECTOR (J9)

Many different panels are supported by the on board graphic controller. Up to sixteen types can be predefined in the graphic BIOS and selected by on board switches (please refer section 3.2.1). Pin names listed in Table 3-9 are for a general overview. They reflect the connection for a 24 bit TFT panel. Some pins may change with different configurations. Signals for controlling panel power, contrast and brightness are also available. All panel interface signals are 3.3V based.

Some of the on board serial peripherals are available on this connector as well. There are the keyboard and mouse interface signals and the RS232 RX/TX signals from the UART1. The USB port1 datasignals can be routed to the connector via assembly option. These signals may be used to connect a Touch Panel or for a complete Man Machine Interface.

It is beyond the scope of this manual to give a complete description of the panel interface of the C&T 69000. Please refer to its documentation or/and contact MPL AG for implementation specific details.

50-pin connector Samtec typ RSM-125-02-L-D (1.27mm pitch) pinout:

Pin number	Signal	B69000 (Note 3)	Pin number	Signal	B69000 (Note 3)
1	RD6	P22	2	RD7	P23
3	RD4	P20	4	RD5	P21
5	RD2	P18	6	RD3	P19
7	RD0	P16	8	RD1	P17
9	GD6	P14	10	GD7	P15
11	GD4	P12	12	GD5	P13
13	GD2	P10	14	GD3	P11
15	GD0	P8	16	GD1	P9
17	BD6	P6	18	BD7	P7
19	BD4	P4	20	BD5	P5
21	BD2	P2	22	BD3	P3
23	BD0	P0	24	BD1	P1
25	First Line Marker	FLM	26	Latch Pulse	LP
27	Shift Clock / Pixel Clock	SHFCLK	28	Display Enable	M/DE/BLANK/ACDCLK
29	CTRL2 (contrast & brightness)	GPIO4	30	CTRL3 (contrast & brightness)	GPIO7
31	+3.3VDC		32	Power Control	ENAVDD
33	+5VDC		34	+5VDC	
35	Keyboard Clock		36	Keyboard Data	
37	Mouse Clock		38	Mouse Data	
39	MPL specific output, do not connect (Note 1)		40	MPL specific input, do not connect (Note 1)	
41	MPL specific input, do not connect (Note 1)		42	Not connected or USB port1 Data+ (Note 2)	
43	Not connected or USB port1 Data- (Note 2)		44	+5VDC	
45	+5VDC		46	+5VDC	
47	+5VDC		48	+5VDC	
49	RS232-RXD1		50	RS232-TXD1	

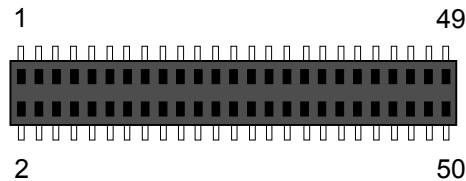
**Table 3-9 Panel & serial Peripherals connector**

Notes:

1. Signal used on MIP520 compatible MPL Panellink Transmitter Module REMMI-T
2. See section 3.2.2 for more details. Default is not connected.
3. These signal names refer the convention of the B69000 user manual

Counterpart is the Samtec connector typ FTR-125-xx-S-D.

Pin numbering on Panel & Serial Peripherals connector:



**3.4.7.1 EASY PANEL AND MAN MACHINE INTERFACE SUPPORT**

For an easy panel connection MPL AG offers adapter boards for different panel types as LVDS panels or 5V panels. Please contact MPL AG or your local distributor for information about supported interfaces and panel types.

For a man machine interface (MMI) support over a distance of up to 10m and more, MPL AG offers a Panellink Transmitter and Receiver Module pair (REMMI-T and REMMI-R). These modules comply to the M3I standard defined by MPL AG. The Transmitter module can be directly mounted to the Panel & serial Peripherals connector (J9) on the MIP520.

The goal of the M3I standard and the implementation in the REMMI family is to offer connection possibilities to standard connectors for the following interfaces in a distance of up to 10m and more.

- PS/2 keyboard and mouse
- One RS232 interface
- One USB port (supports only 6m cable length)

Additionally it offers the following capabilities.

- Panel interface up to 24 bits
- Brightness and contrast control by software and by switches on the panel
- Power supplied to the panel by the MIP520 or by an external power supply

**3.4.7.1.1 BRIGHTNESS AND CONTRAST CONTROL THROUGH THE M3I INTERFACE**

Brightness and contrast control is established by two GPIO pins of the B69000 graphic chip. A special protocol ensures independent control of contrast and brightness with just two digital I/Os. The following table shows the principal of the protocol:

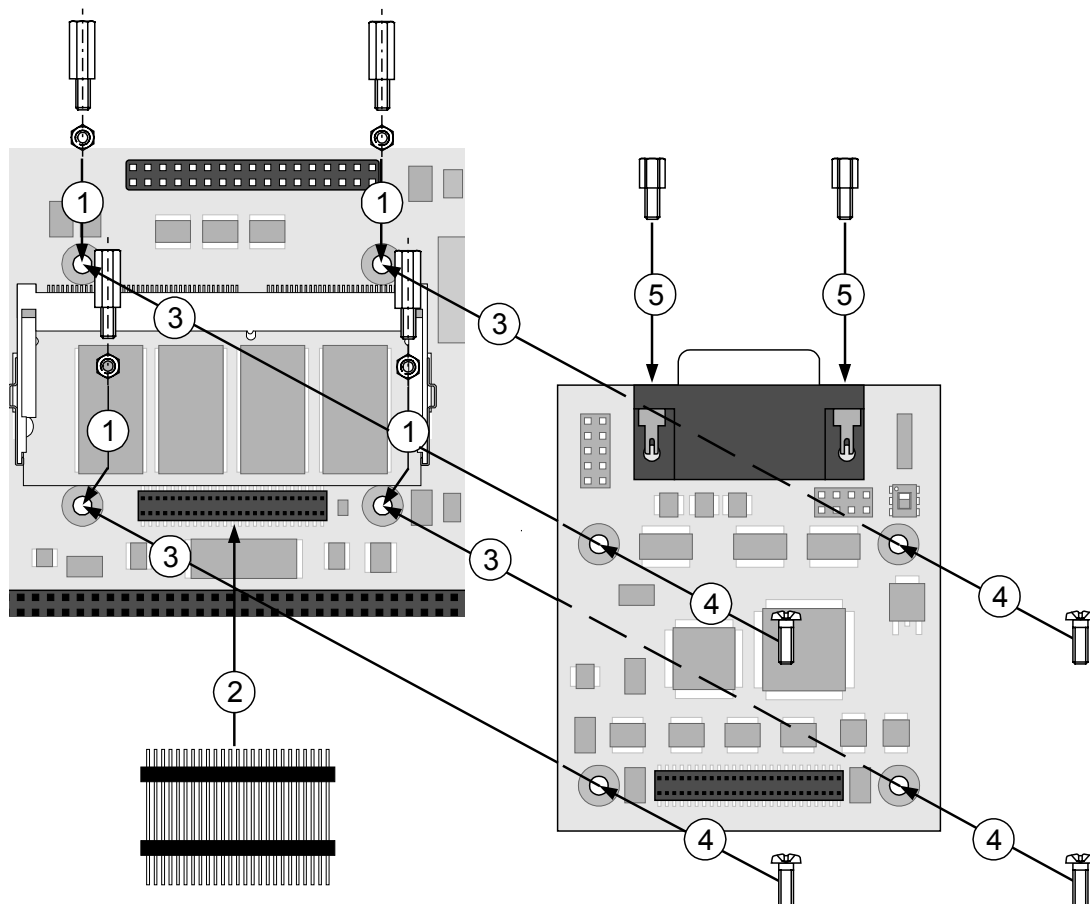
GPIO4	GPIO7	Action
0	0	No change
0	↑ (pos. edge)	Brightness +
0	↓ (neg. edge)	No change
1	↑ (pos. edge)	No change
1	↓ (neg. edge)	Brightness -
↑ (pos. edge)	0	Contrast +
↓ (neg. edge)	0	No change
↑ (pos. edge)	1	No change
↓ (neg. edge)	1	Contrast -
1	1	No change

**Table 3-10 Panel brightness & contrast control protocol**

To avoid uncontrolled behavior, it must be ensured that the time between two transitions from one state to another is greater or equal than 1ms and that the transition from 00 to 11 or vice versa occurs within 20µs.

### 3.4.7.1.2 MOUNTING A PANEL OR MMI MODULE

Before you begin with the module installation, please make sure that no power is applied to the system.



**Figure 3-5 Mounting an MMI module (REMMI-T)**

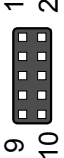
#### **Installation Steps:**

1. Mount the four stacking spacer with nut on the MIP520 (you can also use coupling nuts and screws).
2. Install the board-to-board stacker with the short end into the module socket connector on the MIP520.  
**Please, take care that all contact pins of the board stacker are plugged in correctly and that the connector is installed straight.**
3. After this the module (such as REMMI-T) can be plugged on the mounted board-to-board stacker.
4. Now the module has to be fixed with four screws on the stacking spacers.  
**Important: All four screws must be tightened well since it is the ground connection for the module.**
5. Optionally on REMMI-T two inner thread screws can be fastened on the DSUB connector.
6. Select the desired panel type using DIP Switch1-4..7 (refer to section 3.2.1)

### 3.4.8 CRT CONNECTOR (J2)

The CRT connector is a 10 pin 2mm pitch header.

10 pin CRT header pinout:

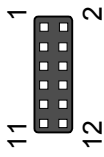
Pin number	Signal Description	Pin number at standard 15 pin HD-DSUB	Pinout
1	Blue	3	
2	Analog Ground	6, 7, 8	
3	Green	2	
4	+5V	9	
5	Red	1	
6	Ground	5, 10	
7	Horizontal synchronization	13	
8	DDC data	12	
9	Vertical synchronization	14	
10	DDC clock	15	

**Table 3-11 CRT connector**

### 3.4.9 SERIAL TTL AND IrDA CONNECTOR (J16)

The serial TTL and IrDA interface connector is a 12 pin 2mm pitch header. From production revision D on, there are two serial interfaces, one usable as infrared interface, on this connector. The signals on both interfaces have TTL level.

12 pin serial TTL and IrDA interface header pinout:

Pin number	Signal	Pinout
1	+5V <sub>DC</sub>	
2	IRRX3	
3	TXD4 or IRTX	
4	RXD4 or IRRX	
5	GND	
6	GND	
7	TXD2 (Note 1)	
8	RXD2 (Note 1)	
9	RTS2 (Note 1)	
10	CTS2 (Note 1)	
11	DTR2 (Note 1)	
12	DSR2 (Note 1)	

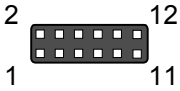
**Table 3-12 Infrared & serial TTL interface**

Note:

1. These assignments are true from production revision D on (see section 7.3).

### 3.4.10 AMDebug / JTAG CONNECTOR (J6)

This 12 pin 2mm pitch header is mainly for MPL internal use only. However, customers requiring access to the debug capabilities of the Élan™SC520 can get it through this connector. Following table shows the pinout:

Pin number	Signal Description	Pinout
1	Ground	
2	Power Good	
3	JTAG Clock	
4	Command Ack	
5	JTAG TMS	
6	BR/TC	
7	JTAG TDI	
8	Stop/TX	
9	JTAG TDO	
10	Trig/Trace	
11	SReset#	
12	Not connected	

**Table 3-13 AMDebug / JTAG connector**

**NOTE**

In order to use the AMDebug interface, a jumper must be placed over Pins 1 and 2 of J7.  
Pins 3 and 4 of J7 must be left open!

To use the debug capabilities of the Élan™SC520 the DIP-switch SW1-2 is needed to Enter the AMDebug mode. And the DIP-switch SW1-3 can be used to enable the Instruction Trace function (see section 3.2.1). There exist several debug tools for the Élan™SC520 from third-party vendors in AMD's FusionE86 program. Some of the run-control tools are listed below:

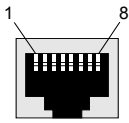
Company	Tool	Internet
CAD-UL	XDB OCDemon for Élan™SC520	<a href="http://www.cadul.com">www.cadul.com</a>
Applied Microsystem Corporation (AMC)	CodeTAP, SuperTAP	<a href="http://www.amc.com">www.amc.com</a>

**Table 3-14 Run-control tools**

**3.4.11 10/100 BASE T/TX CONNECTOR (J3)**

The 10/100 Base T/TX connector is a standard RJ45 connector with integrated magnetics.

8 pin standard RJ45 ethernet pinout:

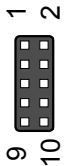
Pin number	Signal	Description	Pinout
1	TX+	Transmit data +	 <p>RJ45</p>
2	TX-	Transmit data -	
3	RX+	Receive data +	
4	NC	Not connected	
5	NC	Not connected	
6	RX-	Receive data -	
7	NC	Not connected	
8	NC	Not connected	

**Table 3-15 10/100 Base T/TX connector**

**3.4.12 USB CONNECTOR (J10)**

The USB connector is a 10 pin 2mm pitch header. It has the signals for two USB ports on it.

10 pin USB header pinout:

Pin number	Signal	Description	Pinout
1	VCC	Cable Power +5VDC Port1	
2	VCC	Cable Power +5VDC Port2	
3	Data1-	Balanced Data Line- Port1	
4	Data2-	Balanced Data Line- Port2	
5	Data1+	Balanced Data Line+ Port1	
6	Data2+	Balanced Data Line+ Port2	
7	GND	Cable Ground Port1	
8	GND	Cable Ground Port2	
9	NC	Not connected	
10	NC	Not connected	

**Table 3-16 USB connector**

### 3.5 WIRING OF CONNECTORS

This section first shows the relations for wiring the 50 pin HD connector J4 to standard interface connectors of the respective interfaces. At the end is an overview of the available easy assembly kits to the MIP520 connectors from MPL AG.

#### 3.5.1 PARALLEL PORT FROM 50-PIN HD CONNECTOR

Wired 1:1 with flat cable from J4 to a standard (female) DB25 flat ribbon IDC connector.

Pin J4	Signal	Pin DB25
1	/Strobe	1
2	/Auto Line Feed	14
3	Data0	2
4	/Error	15
5	Data1	3
6	/Init	16
7	Data2	4
8	/Select In	17
9	Data3	5
10	GND	18
11	Data4	6
12	GND	19
13	Data5	7
14	GND	20
15	Data6	8
16	GND	21
17	Data7	9
18	GND	22
19	/Acknowledge	10
20	GND	23
21	Busy	11
22	GND	24
23	Paper End	12
24	GND	25
25	Select	13

**Table 3-17 Wiring of Parallel Port**

#### 3.5.2 SERIAL PORTS FROM 50-PIN HD CONNECTOR

Wired 1:1 with flat cable from J4 to standard (male) DB9 flat ribbon IDC connectors.

Pin J4 (COM3)	Signal	Pin DB9	Pin J4 (COM1)	Signal	Pin DB9
26	GND	5	35	GND	5
27	RI3	9	36	RI1	9
28	DTR3	4	37	DTR1	4
29	CTS3	8	38	CTS1	8
30	TXD3	3	39	TXD1	3
31	RTS3	7	40	RTS1	7
32	RXD3	2	41	RXD1	2
33	DSR3	6	42	DSR1	6
34	DCD3	1	--	not connected	1

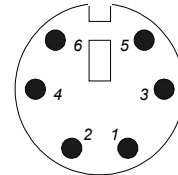
**Table 3-18 Wiring of Serial Ports**

### 3.5.3 PS/2 MOUSE FROM 50-PIN HD CONNECTOR

Wired from J4 to standard 6-pin mini-DIN (female) connector.

Pin J4	Signal	Pin mini-DIN
43	MSDAT	1
-	NC	2
46	GND	3
45	VCC	4
44	MSCLK	5
-	NC	6

**Table 3-19 Wiring of PS/2 Mouse**



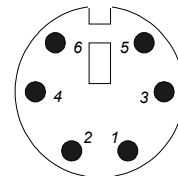
**Figure 3-6 Front view PS/2 Mouse Connector**

### 3.5.4 PS/2 KEYBOARD FROM 50-PIN HD CONNECTOR

Wired from J4 to standard 6-pin mini-DIN (female) connector.

Pin J4	Signal	Pin mini-DIN
47	MSDAT	1
-	NC	2
50	GND	3
49	VCC	4
48	MSCLK	5
-	NC	6

**Table 3-20 Wiring of PS/2 Keyboard**



**Figure 3-7 Front view PS/2 Keyboard Connector**

### 3.5.5 MPL ASSEMBLY KITS FOR MIP520

Below is an overview of the available easy assembly kits to the MIP520 connectors from MPL AG. Please contact MPL AG for further details.

Assembly Kit	Description	for MIP520 connector	Kit output connectors
MPL50-KIT	50 pin high density connector with 1m flat ribbon cable	J4	---
STDPERI-1	Parallel, 2xRS232, KB & Mouse connectors built on PCB; set includes the MPL50-KIT	J4	standard DB25 for Parallel, 2x standard DB9 for Serial, 2x 6pin Mini-DIN for KB & Mouse
MIP-KIT	VGA, USB, speaker & SSI each on PCB with cables to MIP520; RJ45 Gender Changer on PCB	J2 J10 J13 J3	standard 15pin HDSUB for CRT, standard double USB, 2.54mm header for SSI & Speaker, standard RJ45 for Ethernet
485/IrDA-KIT	TTL level signals converted to RS485 and IrDA on PCB with cable to MIP520	J16	DB9 for RS485, IrDA-LED

**Table 3-21 Assembly kits for MIP520 from MPL AG**

### 3.6 APPLYING POWER IN SINGLE BOARD APPLICATIONS

In any case, power to the MIP520 must be applied at PC/104 connector or External Power connector J15. All other connectors which do have power pins as well MUST NOT be used to power the board.

The required supply voltage for the MIP520 is +5V<sub>DC</sub>.

+12V, -12V and -5V are maybe required to supply stacked PC/104 modules, if this voltages are not generated on the PC/104 extension board itself. The MIP520 does not supply this voltages.

## 4. OPERATION

### 4.1 BLOCK DIAGRAM

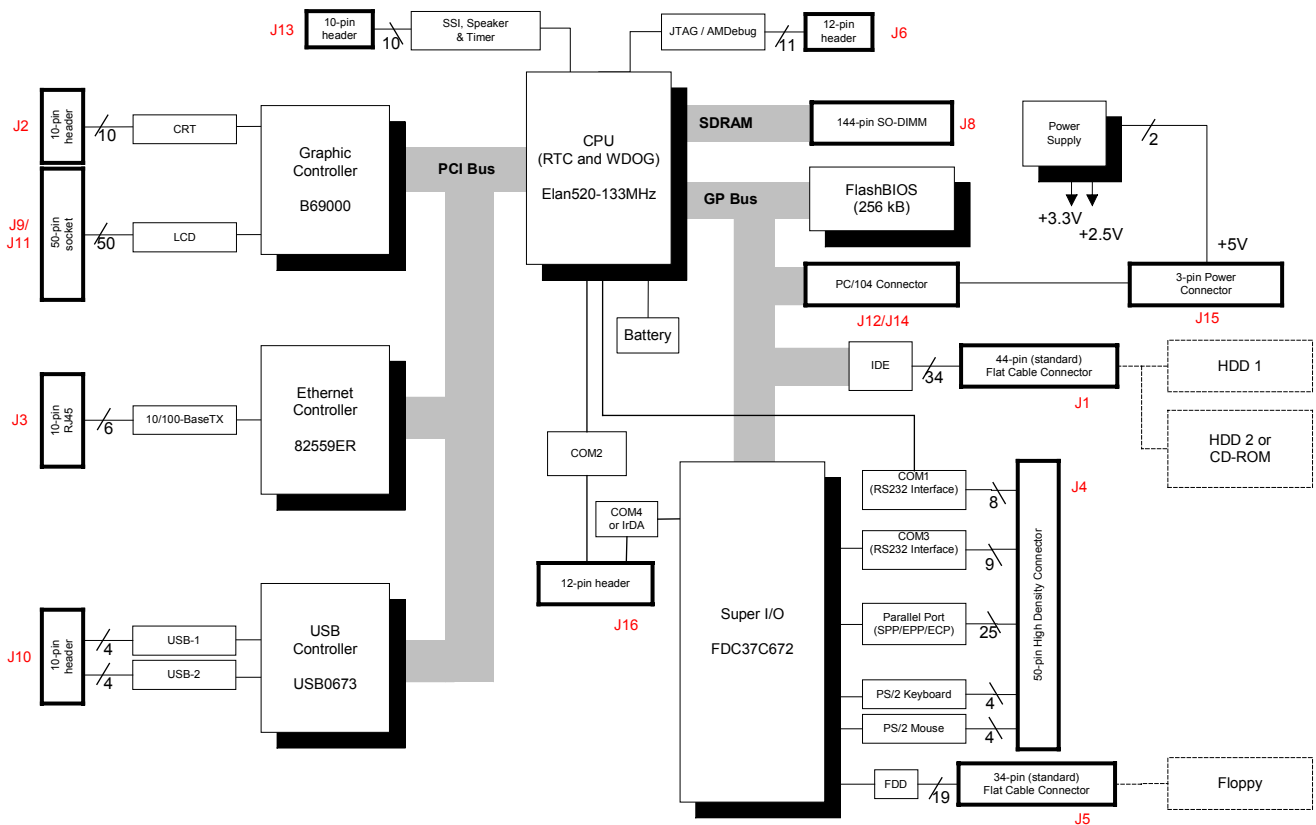


Figure 4-1 MIP520 Block Diagram

### 4.2 PC/AT FUNCTIONALITY

The MIP520 operates as a standard PC/AT with all dedicated registers for:

- Timers
- Interrupt controller
- DMA controller
- Real Time Clock
- Keyboard controller
- Parallel, Serial Ports
- E-IDE controller
- FDD controller
- Graphic controller

### **4.3 STATUS INDICATORS**

The MIP520 provides two status indicator LED's for the LAN part. The LED's are integrated in the RJ45 connector.

#### **4.3.1 LAN LINK AND ACTIVITY INDICATOR LED**

The green LED is lit whenever a valid link exists. When activity is present, the green LED will flash.

#### **4.3.2 LAN 10/100 MBPS INDICATOR LED**

The yellow LED is lit when the network controller is operating in 100 Mbit/s mode.

### **4.4 BATTERY CIRCUIT**

An on board battery is provided to guarantee data retention of RTC and CMOS RAM in power down situations. Battery backup of these functions is enabled at DIP-switch SW1-8 (see section 3.2.1). The battery has a capacity of 170mAh.

## 4.5 PROGRAMMABLE WATCHDOG TIMER

The MIP520 provides an integrated programmable watchdog timer in the Élan™SC520. By default the watchdog is disabled at power up. For reconfiguration and to reset the current count special write sequences are required. The time-out period is programmable between 0.5msec and 32sec. The watchdog can be programmed to either generate a system reset or an interrupt request (maskable or non-maskable) on the first time-out. If the software has not cleared an indicator bit by the second time-out, the watchdog timer always generates a system reset instead.

### 4.5.1 PROGRAMMING THE WATCHDOG

The watchdog is controlled by the memory-mapped registers listed in Table 4-1. All writes to the Watchdog Timer Control (WDMRCTL) register must be preceded by a distinct keyed sequence.

- A data pattern of 3333h, followed by a write of CCCCh, to the WDTMRCTL register opens up the register for a single write (*write key sequence*).
- Setting the bit ENB in the register WDTMRCTL, enables the watchdog timer. The watchdog timer starts counting up.
- While enabled, the software can reset the counter to 0 anytime by writing a data pattern of AAAAh, followed by a write of 5555h, to the WDTMRCTL register (*clear-count key sequence*). This sequence resets the counter and restarts counting up (feeding the watchdog). If the register has not been written within the specified time-out interval a system reset or interrupt will be performed.
- Once the ENB bit is set in the WDTMRCTL register, an other *write key sequence* is required to allow a write to this register.

For the detailed register description please refer the „Élan™SC520 Register Set Manual“.

Register	Mnemonic	MMCR Offset Address	Function
Watchdog Timer Control	WDTMRCTL	CB0h	WD timer enable, reset enable, interrupt flag, duration of time-out interval
Watchdog Timer Count Low	WDTMRCNTL	CB2h	Bits 15-0 of the WD current count
Watchdog Timer Count High	WDTMRCNTH	CB4h	Bits 30-16 of the WD current count
Watchdog Timer Interrupt mapping	WDTMAP	D42h	WD interrupt mapping
Reset status	RESSTA	D74h	Reset source status: WD time-out

**Table 4-1 Watchdog control registers**

## 4.6 SOFTWARE TIMER

The software timer is intended to provide a millisecond timebase with microsecond resolution. Ideal applications for this function include providing a wide software timebase, code profiling, and precise measurement of the time between events.

It is designed to replace the traditional method of system timebase generation with periodic interrupt.

### 4.6.1 USING THE SOFTWARE TIMER

The Software timer provides a 16-bit millisecond-up counter and a latch register for a 10-bit microsecond-up counter. The microsecond-up counter increments at a rate of 1MHz and rolls over on every 1000 counts (every 1 millisecond). When this happens, it signals the millisecond counter to increment. The software timer includes the registers listed below.

Register	Mnemonic	MMCR Offset Address	Function
Software Timer Millisecond Count	SWTMRMILLI	C60h	Current 16-bit count value (milliseconds)
Software Timer Microsecond Count	SWTMRMICRO	C62h	Current latched 10-bit count value (microseconds)
Software Timer Configuration	SWTMRCFG	C64h	Crystal frequency select (on MIP520 – 33.000 MHz)

**Table 4-2 Software Timer registers**

When the millisecond counter is read, three things happen:

1. The value in the Software Timer Millisecond Count register is returned to the software.
2. The value in the microsecond-up counter is latched into the Software Timer Microsecond Count register.
3. The Software Timer Millisecond Count register counter is reset to zero.

This operation allows software to keep track of time with no interrupt service routine. In order to maintain a millisecond time base, the Software Timer Millisecond Count register must be read at least once every 65.5 seconds. At system reset, the software timer begins counting up from zero. [The timer must be initialized for operation with a 33.000 MHz crystal.](#) This is configured with the XTAL\_FREQ bit set to one in the software timer configuration register.

For the detailed register description please refer the „Élan™SC520 Register Set Manual“.

**NOTE**

On some MIP520 is a 32.000MHz crystal mounted due to availability reasons.  
This leads to a small timing difference!

## 4.7 USING PC/AT INTERRUPTS

As every standard PC, the MIP520 provides 17 Hardware interrupt channels. Some of them are accessible on the PC/104 extension bus. It is the user's responsibility to make sure that no hardware conflict occurs due to a wrong interrupt configuration. Please see Table 4-3 for the MIP520 interrupt assignments.

MIP520 hardware interrupt assignment		PC/104	Released for PC/104 use by
NMI	Disabled	Disabled	Hardware adjustment & Elan register setting (Note 1)
IRQ0	System Timer 0	Not available	--
IRQ1	Keyboard	Not available	--
IRQ2	Cascaded interrupts from 2nd PIC (IRQ8-15)	Not available	--
IRQ3	COM2	Disabled	BIOS & Elan register setting
IRQ4	COM1	Disabled	BIOS & Elan register setting
IRQ5	All on board PCI devices (Graphic, Ethernet, USB)	Disabled	BIOS & Elan register setting
IRQ6	Floppy Disk Controller	Available	Super I/O register setting
IRQ7	LPT1	Available	Super I/O register setting
IRQ8	Real-time Clock	Not available	--
IRQ9	ISA-IRQ9	Available	--
IRQ10	COM3 & COM4 (shared IRQ)	Available	Super I/O register setting
IRQ11	ISA-IRQ11	Available	--
IRQ12	PS/2 Mouse	Available	Super I/O register setting
IRQ13	Math Coprocessor	Not available	--
IRQ14	Hard Disk	Available	Hard Disk
IRQ15	ISA-IRQ15	Available	--

**Table 4-3 MIP520 Interrupt assignments through BIOS**

Note:

1. Because the Elan has no NMI-pin a standard IRQ line has to be used for this. Through hardware & BIOS adjustment IRQ9 on the MIP520 can be used as NMI. Please contact your local distributor or MPL AG for further information.

### NOTE

Some of these interrupts may be used for custom applications if the assigned device is not used and not initialized. Disabling may be performed via accessing dedicated registers.

The interrupts of the on board PCI parts (Graphic, USB, Ethernet) will be mapped to IRQ5 through the BIOS. But it is also possible to map these interrupts fix to any IRQ through Élan™SC520 registers. For the detailed register description please refer the „Élan™SC520 Register Set Manual“. The interrupts of the PCI devices are assigned to the Élan™SC520 according to the following table:

Optional Device (assembled on MIP520)	Interrupt input pin on Élan™SC520
Graphic (B69000)	INTC#
Ethernet (82559ER)	INTA#
USB (USB0673)	INTB#

**Table 4-4 Interrupt assignments of the on board PCI-devices**

#### 4.8 USING PC/AT DMA CHANNELS

On the PC/104 extension bus are 7 ISA DMA channels accessible. Because the on board DMA controller in the Élan™SC520 just supports 4 external DMA-channels it is not possible to use all of them together. To give the user the possibility to use any of the 7 ISA-DMA channel each ISA DMA channel can be routed to any of the four external DMA controller channel. This routing is done through the DMA channel 1/0 and 3/2 registers in the EPLD (see section 4.9).

The four external DMA channels are individually configurable for either 8 or 16 bit and can be mapped to any standard DMA channel inside the DMA controller. This configuration is done through internal Élan™SC520 registers. For the detailed register description see „Élan™SC520 Register Set Manual“.

The on board periphery can also use some of the 7 ISA-DMA channels according to Table 4-5. It is the user's responsibility to make sure that no hardware conflict occurs due to a wrong DMA configuration.

ISA DMA channel	PC/104	Also usable by following on board periphery
0	Available	primary IDE DMA channel
1	Available	Super I/O DMA channel 1 (IrDA)
2	Available	Super I/O DMA channel 2 (Floppy)
3	Available	Super I/O DMA channel 3 (Parallel port in ECP mode)
5	Available	--
6	Available	--
7	Available	--

**Table 4-5 Shared ISA DMA channels with on board periphery**

After startup the BIOS configures the DMA-channels as following:

DMA-Controller channel	mapped DMA signal	usable by following periphery	Comment
0	DMA external CH0	IDE and PC/104 ISA DMA CH0	8 bits wide
1	DMA external CH1	IrDA and PC/104 ISA DMA CH1	8 bits wide
2	DMA external CH2	Floppy and PC/104 ISA DMA CH2	8 bits wide
3	DMA external CH3	Parallel in ECP mode and PC/104 ISA DMA CH3	8 bits wide
5	none	none	16 bits wide
6	none	none	16 bits wide
7	none	none	16 bits wide

**Table 4-6 Mapping of DMA controller channels through BIOS**

On the MIP520 DMA transfers are only possible to and from SDRAM. No transfers are possible to PCI, ROM or peer ISA bus devices!

## 4.9 EXTENSION REGISTERS

The extension registers listed in section 4.9.1 to 4.9.6 are implemented in the on board EPLDs, they are 8 bits wide. The address space of the chip select can be programmed via a Programmable Address Region (PAR) register in the Élan™SC520. Through the MIP520-BIOS the base address for the EPLD is set to IO address 0x800h.

### 4.9.1 PLD ID AND REVISION REGISTER MISC-EPLD

#### MISC-PID/PREV: Offset address 00h (Read Only)

This register is used to identify the code version and revision of the programmable on board MISC-EPLD.

Bit	7	6	5	4	3	2	1	0
Function	PLD Version				PLD Revision			

Table 4-7 MISC PLD ID & Revision register

### 4.9.2 DMA CHANNEL 1/0 MAPPING REGISTER

#### DMA-CH1/0: Offset address 01h (Read/Write)

This register is used to define which ISA-DMA channel is mapped to the DMA controller external channel 0 and channel 1.

Bit	7	6	5	4	3	2	1	0
Function	Not used	DMA12	DMA11	DMA10	Not used	DMA02	DMA01	DMA00
Default	0	0	0	1	0	0	0	0

Table 4-8 DMA Channel 1/0 register

#### DMA0[2..0] (Read/Write)

These bits determine which ISA-DMA channel is routed to the DMA controller external channel 0.

DMA0[2..0]	ISA-DMA
0 0 0	Channel 0 (default)
0 0 1	Channel 1
0 1 0	Channel 2
0 1 1	Channel 3
1 0 1	Channel 5
1 1 0	Channel 6
1 1 1	Channel 7
else	disabled

#### DMA1[2..0] (Read/Write)

These bits determine which ISA-DMA channel is routed to the DMA controller external channel 1.

DMA1[2..0]	ISA-DMA
0 0 0	Channel 0
0 0 1	Channel 1 (default)
0 1 0	Channel 2
0 1 1	Channel 3
1 0 1	Channel 5
1 1 0	Channel 6
1 1 1	Channel 7
else	disabled

### 4.9.3 DMA CHANNEL 3/2 MAPPING REGISTER

#### DMA-CH3/2: Offset address 02h (Read/Write)

This register is used to define which ISA-DMA channel is mapped to the DMA controller external channel 2 and channel 3.

Bit	7	6	5	4	3	2	1	0
Function	Not used	DMA32	DMA31	DMA30	Not used	DMA22	DMA21	DMA20
Default	0	0	1	1	0	0	1	0

**Table 4-9 DMA Channel 3/2 register**

#### DMA2[2..0] (Read/Write)

These bits determine which ISA-DMA channel is routed to the DMA controller external channel 2.

DMA2[2..0]	ISA-DMA
0 0 0	Channel 0
0 0 1	Channel 1
0 1 0	Channel 2 (default)
0 1 1	Channel 3
1 0 1	Channel 5
1 1 0	Channel 6
1 1 1	Channel 7
else	disabled

#### DMA3[2..0] (Read/Write)

These bits determine which ISA-DMA channel is routed to the DMA controller external channel 3.

DMA3[2..0]	ISA-DMA
0 0 0	Channel 0
0 0 1	Channel 1
0 1 0	Channel 2
0 1 1	Channel 3 (default)
1 0 1	Channel 5
1 1 0	Channel 6
1 1 1	Channel 7
else	disabled

#### 4.9.4 MISCELLANEOUS REGISTER

##### MISC: Offset address 03h (Read/Write)

This register is used for controlling a BIOS update.

Bit	7	6	5	4	3	2	1	0
Function	RES	RES	RES	RES	User Switch2	User Switch1	Serial Console	PBIOS
Default	0	0	0	0	X	X	X	0

**Table 4-10 Miscellaneous register**

##### PBIOS (Read/Write)

This bit is used for the programming mode of the on board BIOS flash device.

***This bit must not be set during normal operation !***

PBIOS	Function
0	Normal Operation
1	Programming Mode

##### Serial Console (Read)

This bit shows the value of DIP-switch SW1-1, see section 3.2.1. This switch is used for serial console redirection. If ON (bit 1 value = 0) the standard keyboard and VGA is redirected to serial interface COM1! Allowing access to the MIP520 via an external terminal.

##### User Switch1/2 (Read)

This bits show the value of DIP-switches SW1-6/7, see section 3.2.1. This DIP-switches are also used for defining the panel type. By an assembly option they can be used as user switches only, please contact MPL for more details.

#### 4.9.5 MUX REGISTER

##### MUX: Chipselect EPLD and Register address 04h (Read/Write)

This register is used to adjust the right DQM-muxing control signal for the SDRAM memory module.

Bit	7	6	5	4	3	2	1	0
Function	RES	RES	RES	RES	RES	RES	DQM-MUX1	DQM-MUX0
Default	0	0	0	0	0	0	0	0

**Table 4-11 DQM-Mux register**

##### DQM-MUX[1..0] (Read/Write)

This bits determine which signal is used for controlling the DQM muxing for the SDRAM memory module. The value of the control signal is used for switching the Elan DQM[3..0] to ether SDRAM DQM[3..0] or DQM[7..4].

***This bits are set through the BIOS at startup and must not be changed during normal operation !***

DQM-MUX[1..0]	DQM-Muxing control signal	Comment
0 0	no muxing	Elan SDQM[3..0] fix to SDRAM DQM[3..0]; SDRAM DQM[7..4] always high
0 1	MA11	
1 0	MA12	
1 1	BA1	

**4.9.6 PLD ID AND REVISION REGISTER MUX-EPLD**

**MUX-PID/PREV: Chipselect EPLD and Register address 05h (Read Only)**

This register is used to identify the code version and revision of the programmable on board MUX-EPLD

Bit	7	6	5	4	3	2	1	0
Function	Not implemented (1) (1)		PLD Version		PLD Revision			

**PLD ID & Revision register MUX\_EPLD**

**4.10 EMC FEATURES**

The MIP520 provides all aspects of quality demanded of an industrial computer system. Development according to EMC requirements supports the user in achieving the CE conformity on the system level. This covers features like on board protection and filter devices on power and I/O lines as well as a carefully designed layout.

In a system design, two aspects regarding EMI must be observed. These aspects are immunity to (external) disturbances and prevention of Radio Frequency emissions (RF). On the MIP520, both aspects are taken into account.

Some immunity is given for free since many components do already contain internal circuits providing at least minor protection to ESD. However, special protection devices are provided at exposed locations. As a side effect, the load capacitance of these devices also reduces RF emission slightly.

Immunity and RF emission is kept to a minimum by the 10-layer PCB design. The arrangement of the power planes is lowering the board impedance and improving the RF behavior.

RF emissions are additionally kept low by the use of series resistors in clock and high speed lines. Several interface signals contain special filter devices to reduce emitted radiation.

The table below gives an overview over the ESD protected interfaces and the appropriate I/O pins. The protection levels are taken from the corresponding data sheets and do not represent actual measurements.

Interface	I/O Pins	Level	Condition
RS-232 Interface	RS-232 lines	± 8 kV	IEC 1000-4-2, contact discharge
Parallel Interface	All signals	± 4 kV	Human body model, MIL-STD-883, method 3015
CRT Interface	All data signals	± 8 kV	IEC-61000-4-2, level 4, contact discharge
USB Interface	All data signals	± 4 kV	Human body model, MIL-STD-883, method 3015

**Table 4-12 ESD Protection**

**NOTE**  
 Stated protection levels may only be achieved by properly grounding the MIP520!

## **5. PERFORMANCE**

### **5.1 1<sup>st</sup> LEVEL CACHE**

The CPU has 16kByte cache which is configurable for either write-back or write-through mode. This can be done through BIOS setting in the 'Custom Configuration' screen.

The Élan™SC520 does not have the control mechanism to support an L2 cache.

#### **5.1.1 CACHEABLE AREA**

Caching is controlled by the memory management subsystem, GP bus and PCI bus accesses are not cached. The programmer has control over which regions of memory (SDRAM and ROM) are cacheable and which are not. This is described in the section "System Address Mapping" of the Élan™SC520 User's Manual.

### **5.2 HDD PERFORMANCE**

The MIP520 is able to run HDDs with PIO Mode 0 to 2. Experience showed that some Hard Disk Drives are not able to run in the fastest PIO mode even if they express to do so. Shortening the Hard Disk cable then might be an solution.

## 6. SOFTWARE

### 6.1 BIOS

The MIP520 is equipped with an embedded BIOS from General Software. MPL AG has access to the full source code thus enabling tailoring of the BIOS for special needs.

#### 6.1.1 BIOS UPDATE

The system BIOS of the MIP520 resides in a FLASH memory. Therefore BIOS upgrading with an additional utility is easily possible. For BIOS upgrading, DOS has to be loaded first without any protected mode drivers loaded (e.g., EMM386.EXE). Then start the BIOS upgrade utility "flasher.exe" with the BIOS binary file named as command line parameter:

**C:\flasher [filename]**

After a successful update of the BIOS, please reboot the system.

#### CAUTION

If something fails (e.g., loss of power) during BIOS upgrading (specially after erasing the Flash) and the utility is not able to terminate properly, the MIP520 will no longer have a valid BIOS!  
In these cases, contact MPL AG to start up the system again.

#### 6.1.2 BIOS RELEASE INDEX

The BIOS release index is shown during boot and appears as follows:

MPL MIP520 BIOS **V1.00** (Rev. D)

**Note:**

**V0.2x** are from BIOS releases that have to be used for MIP520 Rev. A and Rev. B devices.  
Please do not use BIOS V0.2x for MIP520 Rev.D (or above) !

**V0.3x** are from BIOS releases that have to be used for MIP520 Rev. C devices.  
Please do not use BIOS V0.3x for MIP520 Rev.D (or above) !

**V1.xx** are the BIOS releases that have to be used for MIP520 Rev.D (or above) devices.  
Please do not use BIOS V1.xx for MIP520 Rev. A..C !

V1.00 is the current BIOS release index (may have been changed in the meantime).  
All the following descriptions reflect BIOS Rev. 1.00.

### 6.1.3 BIOS SCREEN - Custom Configuration

'Custom Configuration' setup allows the configuration of MIP520 specific hardware. Some of the adjustable settings are explained below.

#### 6.1.3.1 COM2 SPEED

The UART2 can work with baud rates up to 1.152 Mbps. The given COM2 interface on the MIP520 works with TTL level, if you connect an external serial driver do NOT go beyond those maximum baud rates!

<b>COM2 Speed</b>	Selects the UART2 clock frequency (1.8432MHz or 18.432 MHz)	
Default	<i>max 115.2 kbps</i>	UART clock 1,8432 MHz for baud rates of up to 115,2 kbps (normal operation)
	<i>max 1.152 Mbps</i>	UART clock 18,432 MHz for baud rates of up to 1,152 Mbps (highspeed operation)

#### 6.1.3.2 COM4 MODE

The UART4 on the MIP520 can be used also as infrared interface instead of a standard serial interface. If it works in infrared mode use the IRRX, IRTX, IRRX3 and the power pins on the 'Serial TTL & IrDA' connector to adapt an external infrared transceiver. For Fast IR (special mode of IrDA) use a transceiver with a second receive data channel (IRRX3).

<b>COM4 Mode</b>	Selects UART4 working mode	
Default	<i>standard UART</i>	UART4 works as standard UART at baud rates up to 115,2 kbps.
	<i>IrDA IR</i>	UART4 works as infrared interface in Fast Infrared (FIR) mode at baud rates up to 4 Mbps.
	<i>ASK IR</i>	UART4 works as infrared interface in Amplitude Shift Keyed (ASK) mode at baud rates up to 19.2 kbps.

#### 6.1.3.3 PARALLEL PORT FLOPPY

The SIO used in the MIP520 allows to use the standard parallel port as external floppy disk port. With this setting you can change the parallel port mode.

<b>Parallel Port Floppy</b>	Selects the parallel port operating mode	
Default	<i>Disabled</i>	Parallel Port connector uses 'Parallel Port Mode' pin configuration. The Parallel Port operates as <b>standard LPT</b> .
	<i>Enabled</i>	The Parallel Port connector uses 'Floppy Disk Mode' pin configuration. If <i>Parallel Port FDD</i> mode is enabled, the FDD signals are redirected to the Parallel Port connector and an external Floppy Disk Drives can be connected to the LPT port. The original Parallel Port functionality is not available any more. <i>A floppy connected to the standard FDD connector does not work as long as Parallel Port FDD mode is enabled!</i>

#### 6.1.3.4 IDE MODE

Per default the on board IDE connector (J1) is setup as primary IDE port. Allowing to connect up to two IDE drives in master/slave mode. With this setting the user gets the possibility to disable the on board IDE connector in case there exists an other primary IDE port in the system.

<b>IDE Mode</b>	Selects the desired memory base address	
Default	<i>Primary</i>	On board IDE connector is setup as primary IDE port.
	<i>Disabled</i>	On board IDE connector is disabled.

### 6.1.3.5 MEMORY WINDOW ON PC104

To get memory accesses routed to the PC104 a memory window has to be defined on the MIP520. This is done with the following two settings:

<b>MemWin Base</b>	Selects the desired memory base address	
Default	<i>Disabled</i>	No memory window on PC104.
	<i>D 0000h</i>	Memory window at PC104 from base address D0000h on. (max. 32k)
	<i>D 4000h</i>	Memory window at PC104 from base address D4000h on. (max. 32k)
	<i>D 8000h</i>	Memory window at PC104 from base address D8000h on. (max. 16k)
	<i>D C000h</i>	Memory window at PC104 from base address DC000h on. (max. 8k)

<b>MemWin Size</b>	Selects the desired memory size of the window (kB)	
	<i>4</i>	The memory window at PC104 is 4 Kbytes width.
	<i>8</i>	The memory window at PC104 is 8 Kbytes width.
Default	<i>16</i>	The memory window at PC104 is 16 Kbytes width.
	<i>32</i>	The memory window at PC104 is 32 Kbytes width.

**Note:** It is only possible to generate a memory window from D0000h to DF000h, because of standard PC architecture with Élan™SC520! The BIOS will NOT allow you to generate a memory window exceeding this limits.

## 6.2 DEVICE DRIVERS

Drivers for different operating systems are available.

### 6.2.1 LINKS TO THE LATEST DRIVERS

The latest driver versions are also available on the internet.

- INTEL GD82559ER FAST ETHERNET CONTROLLER:  
<http://www.intel.com/design/network/drivers>
- CHIPS & TECHNOLOGY 69000 GRAPHIC CONTROLLER:  
<http://www.asilant.com/driver.htm>
- SMSC FDC37C67x

SMSC IrDA NDIS 5.0 Driver for Windows 98, Windows 98SE,  
Windows Me, and Windows 2000 IrDA drivers  
<http://www.smsc.com/main/tools/ircc/irndisk.zip>

**Note:**

Links may have been changed in the meantime.

The latest links can also be found on the MPL homepage <http://www.mpl.ch/>

## 7. SUPPORT INFORMATION

### 7.1 MPL AG

In case of questions contact your local distributor or MPL AG:

MPL AG homepage: [www.mpl.ch](http://www.mpl.ch)  
Email address: [support@mpl.ch](mailto:support@mpl.ch)

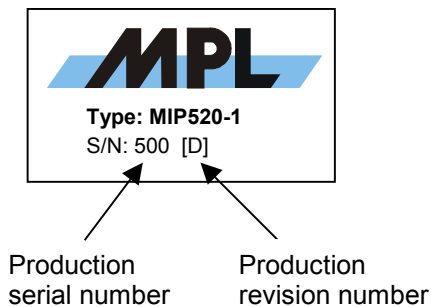
### 7.2 RELATED DOCUMENTS

The high integration level of equipped components offers a lot more features than could possibly be described within the scope of this manual. Several data books related to all the different components are available either directly from the respective manufacturer or distributor or by downloading from the manufacturers Internet site.

However, in most cases these documents are not needed when integrating the MIP520 as a standard PC with an operating system running in a PC-environment. Integrators who want to go beyond these standard capabilities are encouraged to contact their local distributor or email to [info@mpl.ch](mailto:info@mpl.ch).

### 7.3 PRODUCTION NUMBERS

To get the actual production and revision number of your board, please see the label on the bottom of the MIP520 placed on the Élan™SC520:



### 7.4 MISCELLANEOUS CONNECTORS

To facilitate the connection to the different connectors on the MIP520 MPL AG provides some assembly kits, please see section 3.5.5, Table 3-21 Assembly kits for MIP520 from MPL AG.

## 7.5 DISTRIBUTOR ADDRESSES

If the user likes to order connectors and cables from a distributor, a choice of manufacturers with the respective part number is given below:

### 7.5.1 CONNECTOR FOR PARALLEL-, SERIAL-, MOUSE- AND KEYBOARD PORT

- MIP520 on board connector:

**HIROSE** Electric Co., Ltd.

Series: HIF6 "Mini-Flex"  
Part number: HIF6A-50PA-1.27DS

- Counterpart connector:

**HIROSE** Electric Co., LTD

Series: HIF6 "Mini-Flex"  
Part number: HIF6-50D-1.27R

or

**ASSMANN** Electronic Components

Series: Multiflex "High-Density"  
Part number: AWP 50-HD

### 7.5.2 CONNECTOR FOR EXTERNAL POWER

- MIP520 on board connector:

**PHOENIX** Contact AG

Series: MINI-COMBICON  
Part number: MC1,5/3-G-3.81

- Counterpart connector:

**PHOENIX** Contact AG

Series: MINI-COMBICON Plugs, Pitch 3.81mm  
Part number: Depends on customer needs

### 7.5.3 LCD CONNECTOR

- MIP520 on board connector:

**SAMTEC** Inc.

Series: RSM series  
Part number: RSM-125-02-L-D

- Counterpart connector:

**SAMTEC** Inc.

Series: FTR, HTMS, HDWM, DWM, TML, ZML, TMS series  
Part number: Depends on customer needs

#### 7.5.4 2MM CONNECTORS

- MIP520 on board connectors:

**SAMTEC** Inc.

Series: TMM series  
Part number: TMM-10x-02-L-D-MW

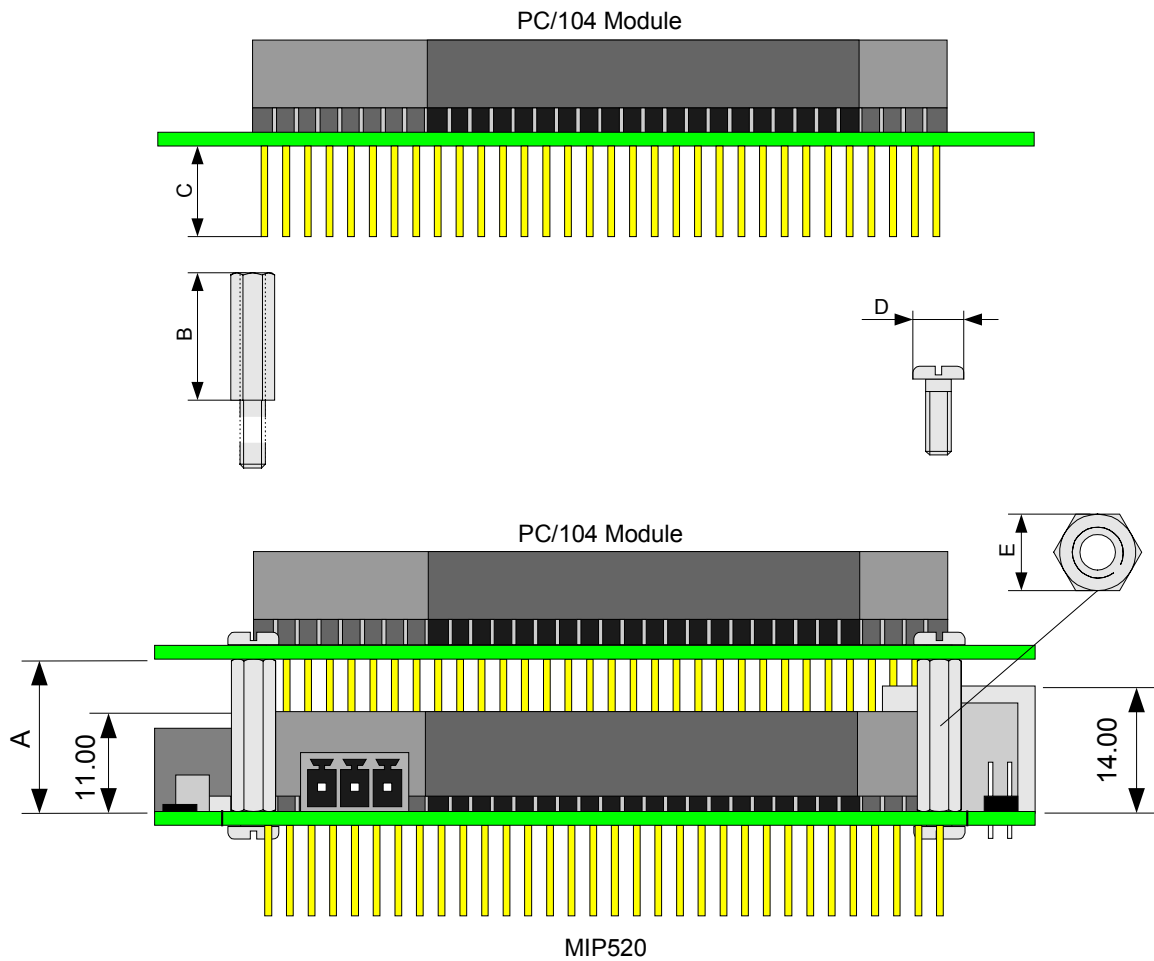
- Counterpart connector:

**SAMTEC** Inc.

Series: TCSD, SMM, SQT, SQW, MMS series  
Part number: Depends on customer needs

## 8. APPENDIX

### 8.1 MOUNTING PC/104 EXTENSION CARDS



**Figure 8-1 PC/104 Stack**

### 8.1.1 SPECIFICATION OF MOUNTING MATERIAL

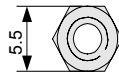
To prevent from electrical short circuits, it is recommended to use synthetic mounting material, such as polyamide screws and nuts. Otherwise isolation washers are needed.

- HEX Coupling Nut  
A: 18mm (standard)  
E: 6.0mm  
Thread: M3 (3mm)

If  $C < 10.7\text{mm}$  (PC/104 standard) it is possible to reduce A to 15.5mm. Be careful not to build a short circuit at the PC/104 module through the RJ45 connector housing. C has to be 7.5mm at least.

- Pan Head or Cylinder Head Machine Screw  
D:  $< 5.5\text{mm}$   
Thread: M3 (3mm)
- Stacking Spacer for additional PC/104 boards  
B: 15mm  
Thread: M3 (3mm)

If Stacking Spacers with nuts are used for the first PC/104 board, please note that for the nut on the bottom side of MIP520 max. 5.5mm wrench opening is recommended.



**Figure 8-2 Bottom side nut**

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<b>Revision Index</b>	<b>Date</b>	<b>Comment</b>
Rev. A	02.03.2001	Created for MIP520 Board revision A,B
Rev. B	26.04.2001	General update of documentation
Rev. C	24.07.2001	Changes because of new MIP520 board revision C
Rev. D	17.10.2001	New interrupt assignments with new BIOS V1.06

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